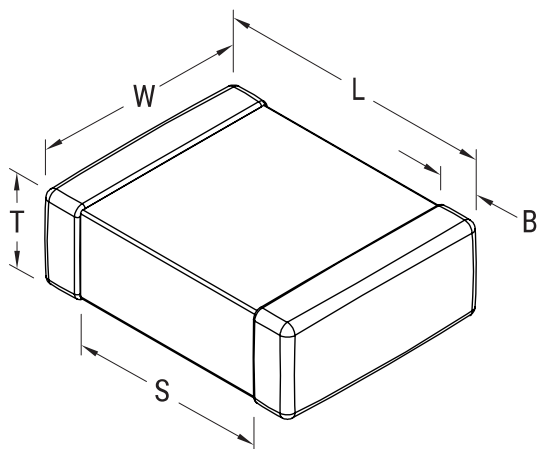


C1210C226M9PACTU

Aliases (C1210C226M9PAC7800)

SMD Comm X5R, Ceramic, 22 uF, 20%, 6.3 VDC, X5R, SMD, MLCC, Temperature Stable, Class II, 1.5 mm, 1210 / 3225



Click [here](#) for the 3D model.

General Information

类别	SMD Comm X5R
样式	SMD Chip
描述	SMD, MLCC, Temperature Stable, Class II
特征	Temperature Stable, Class II
RoHS	Yes
端子	Tin
标记	No
典型元件重量	135 mg
保质期	78 Weeks
MSL	1

Specifications

容值	22 uF
测量条件	120 Hz 0.5Vrms
容差	20%
直流电压	6.3 VDC
耐压电压	15.75 VDC
温度范围	-55/+85°C
温度系数	X5R
电容变化 (相对于+25°C, 0 VDC) (TCC)	15%, 120Hz 0.5Vrms
损耗因数	10% 120 Hz 0.5Vrms
老化率	5% Loss/Decade Hour: Referee Time is 48 Hours
绝缘阻抗	4.5 MOhms

Dimensions

L	3.2mm +/-0.3mm
W	2.5mm +/-0.3mm
T	2.5mm +/-0.30mm
S	1.5mm MIN
B	0.5mm +0.4/-0.25mm
Chip Size / Footprint	1210 / 3225

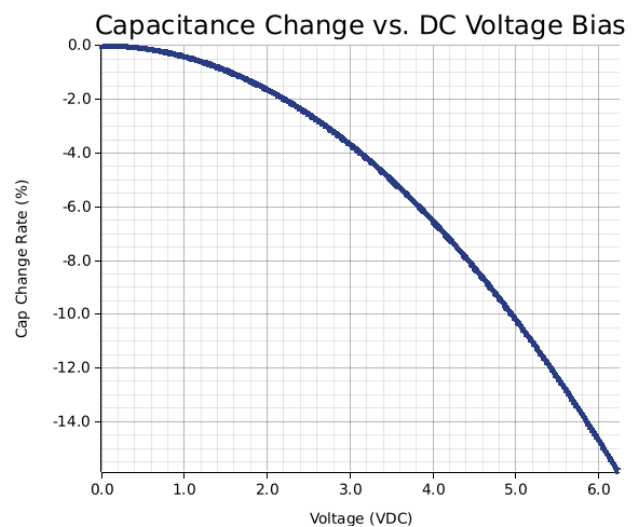
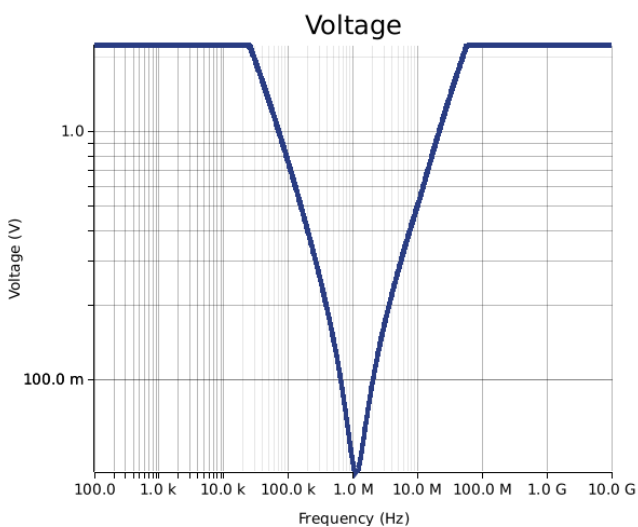
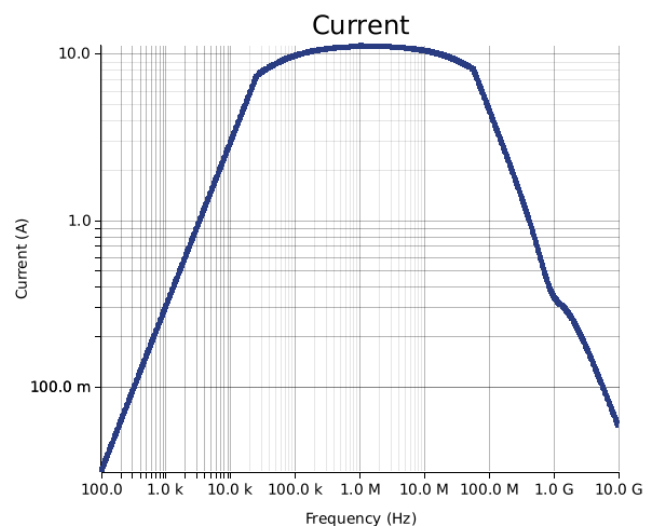
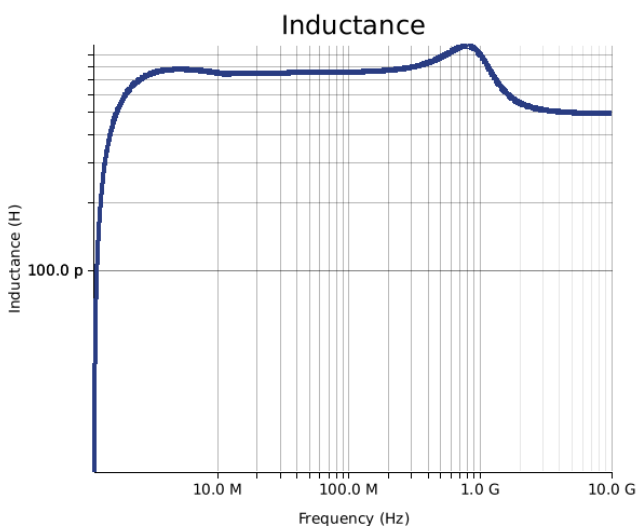
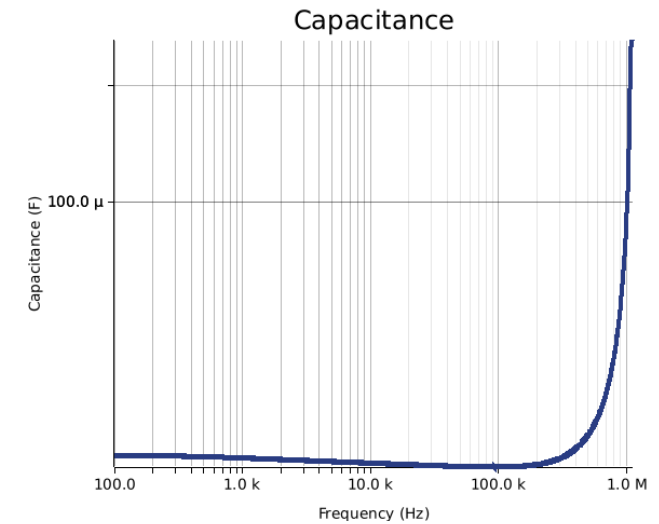
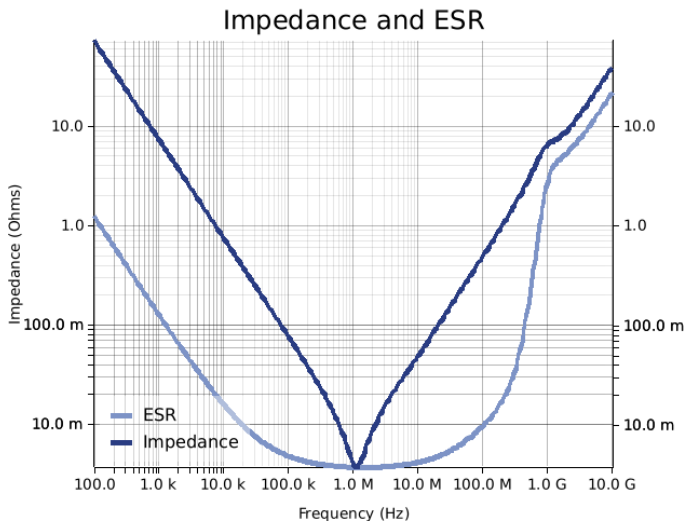
Packaging Specifications

包装	T&R, 180mm, Plastic Tape
包装数量	1000

Statements of suitability for certain applications are based on our knowledge of typical operating conditions for such applications, but are not intended to constitute - and we specifically disclaim - any warranty concerning suitability for a specific customer application or use. This Information is intended for use only by customers who have the requisite experience and capability to determine the correct products for their application. Any technical advice inferred from this Information or otherwise provided by us with reference to the use of our products is given gratis, and we assume no obligation or liability for the advice given or results obtained.

Simulations

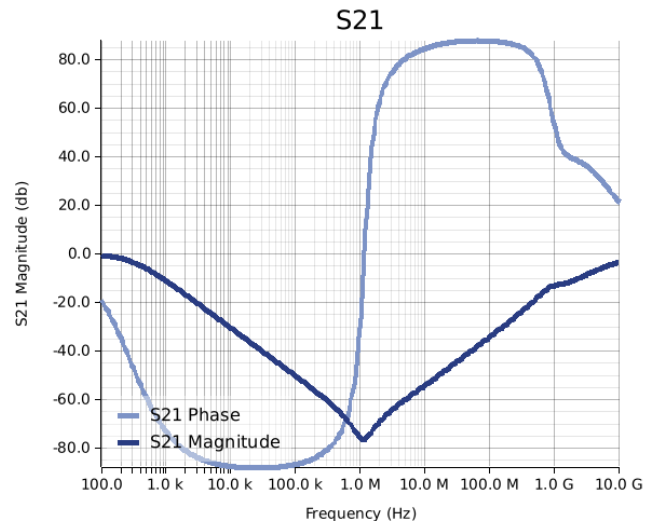
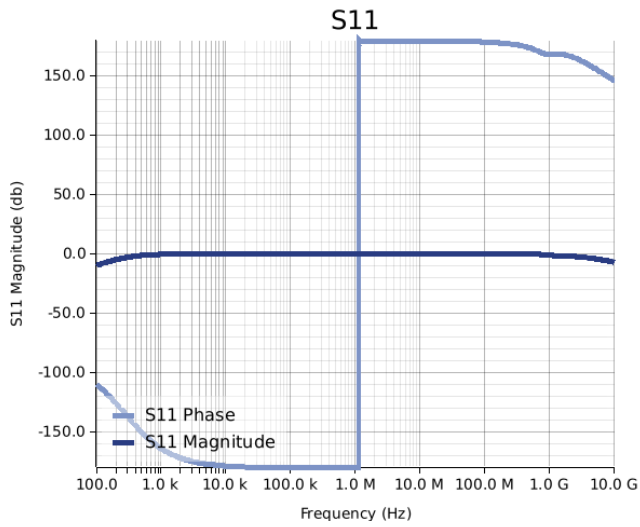
For the complete simulation environment please visit [K-SIM](#).



C1210C226M9PACTU

Aliases (C1210C226M9PAC7800)

SMD Comm X5R, Ceramic, 22 uF, 20%, 6.3 VDC, X5R, SMD, MLCC,
Temperature Stable, Class II, 1.5 mm, 1210 / 3225



These are simulations.

This is not a specification!

The responses shown represent the typical response for each part type. Specific responses may vary, depending on manufacturing variation affects of all parameters involved, including the specified tolerances applied to capacitance and unspecified variations of ESR, ESL, and leakage resistance.

The responses shown do not represent a specified or implied maximum capability of the device for all applications.

- The ESR used for ripple "Ripple Current/Voltage vs. Frequency" plots is the ESR at ambient temperature.
- The ESR in the "Temperature Rise vs. Ripple Current" plots is adjusted to each incremental temperature rise before the power and ripple current is calculated.
- The effects shown herein are based on measured data from a multiple part sample of the parts in question.
- Ripple capability of this device will be factored by thermal resistance (Rth) created by circuit traces (addi affects of all parameters involved, including the specified tolerances applied to capacitance and unspecified variations of ESR, ESL, and leakage resistance.
- The peak voltages generated in the "Temperature Rise vs. Combined Ripple Currents" plot are calculated for each frequency and are not combined with voltages generated at any other harmonics.
- Please consult with the catalog or field applications engineer for maximum capability of the device in specific applications.

All product information and data (collectively, the "Information") are subject to change without notice.

KEMET K-SIM is designed to simulate behavior of components with respect to frequency, ambient temperature, and DC bias levels. The responses shown represent the typical response for each part type. Specific responses may vary, depending on manufacturing variation effects of all parameters involved, including the specified tolerances applied to capacitance and unspecified variations of ESR, ESL, and leakage resistance.

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If you have any questions please contact K-SIM.