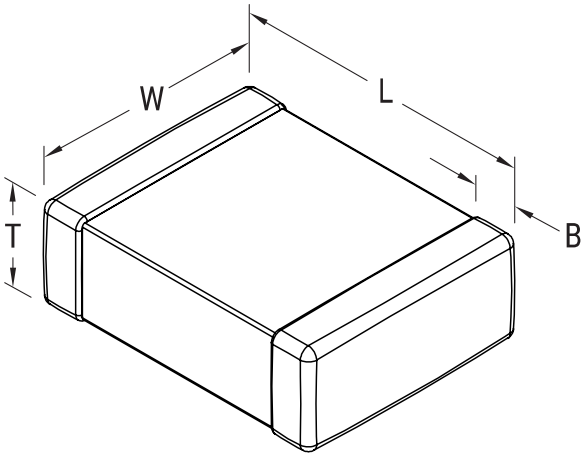
# CQ0402JRNP09BN101

CQ, Ceramic, 100 pF, 5%, 50 VDC, C0G, 0402 / 1005




Click here for the 3D model.

| General Information | |
|---|---|
| Series | CQ |
| Style | SMD Chip |
| Features | Ultra High Q, Low ESR, Class I |
| RoHS | Yes |
| Termination | Tin |

| Dimensions | |
|---|---|
| L | 1mm +/-0.05mm |
| W | 0.5mm +/-0.05mm |
| T | 0.5mm +/-0.05mm |
| B | 0.25mm +/-0.100mm |
| Case Code (EIA / mm) | 0402 / 1005 |

| Packaging Specifications | |
|---|---|
| Packaging | T&R, 178mm, Paper Tape |
| Packaging Quantity | 10000 |

| Specifications | |
|---|---|
| Capacitance | 100 pF |
| Tolerance | 5% |
| Voltage DC | 50 VDC |
| Temperature Range | -55/+125°C |
| Temp. Coefficient | C0G |
| Dissipation Factor | 0.1% |
| Insulation Resistance | 10 GOhms |
| Endurance (% Rated voltage) | 200% |

Statements of suitability for certain applications are based on our knowledge of typical operating conditions for such applications, but are not intended to constitute - and we specifically disclaim - any warranty concerning suitability for a specific customer application or use. This Information is intended for use only by customers who have the requisite experience and capability to determine the correct products for their application. Any technical advice inferred from this Information or otherwise provided by us with reference to the use of our products is given gratis, and we assume no obligation or liability for the advice given or results obtained.



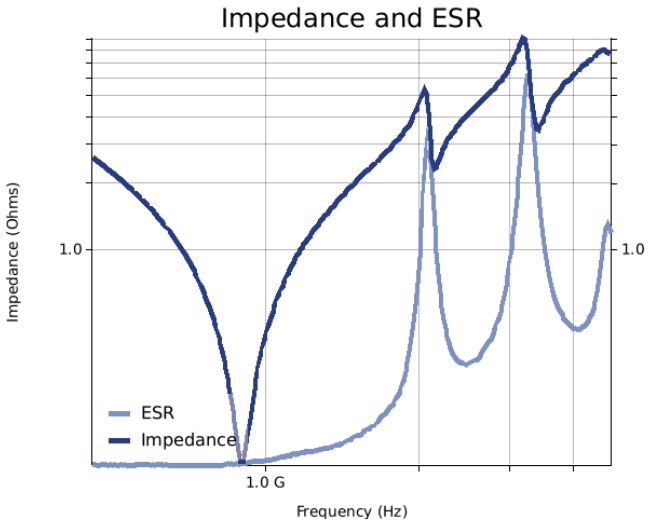
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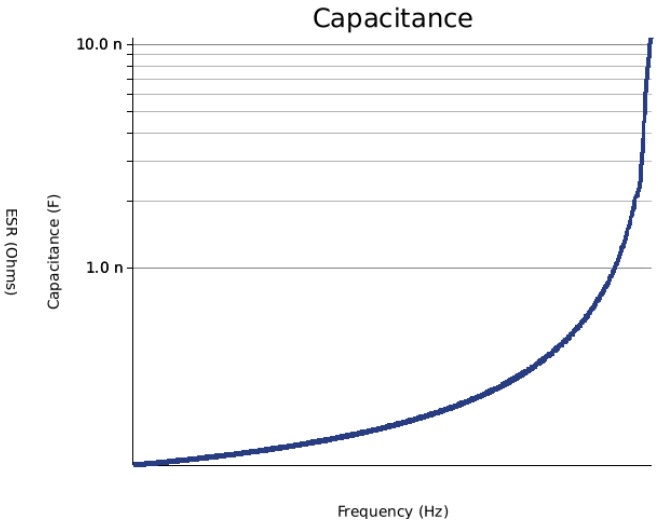
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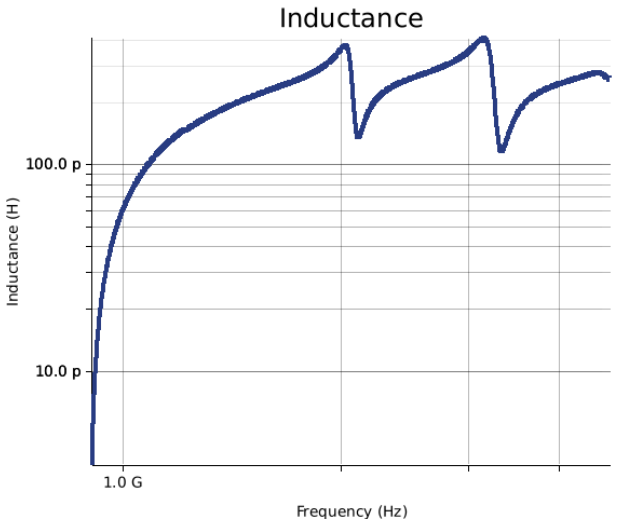
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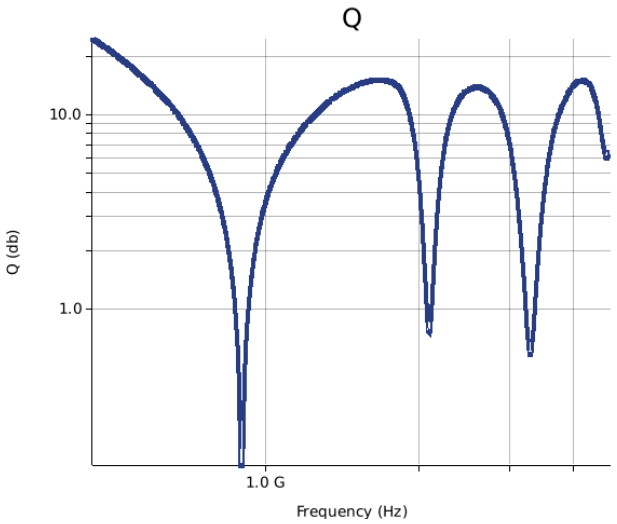
## Simulations

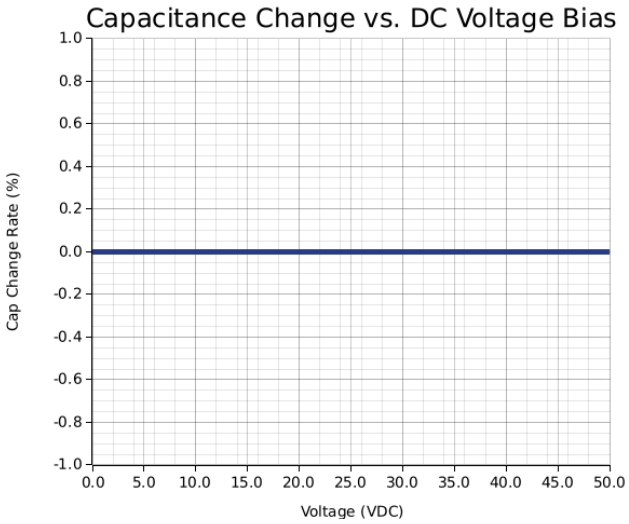
For the complete simulation environment please visit Y-SIM.

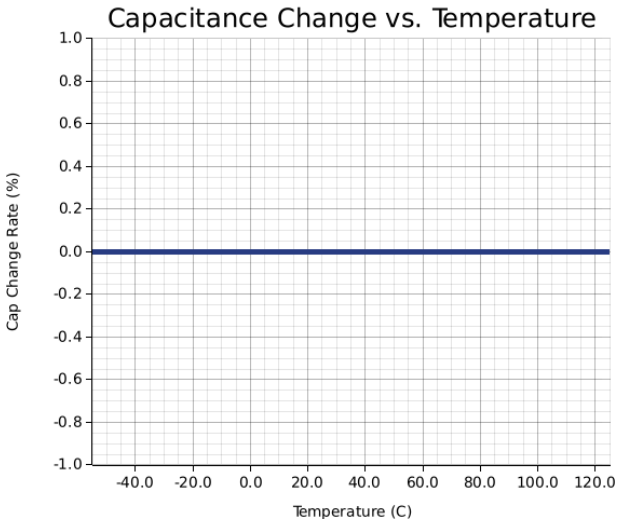


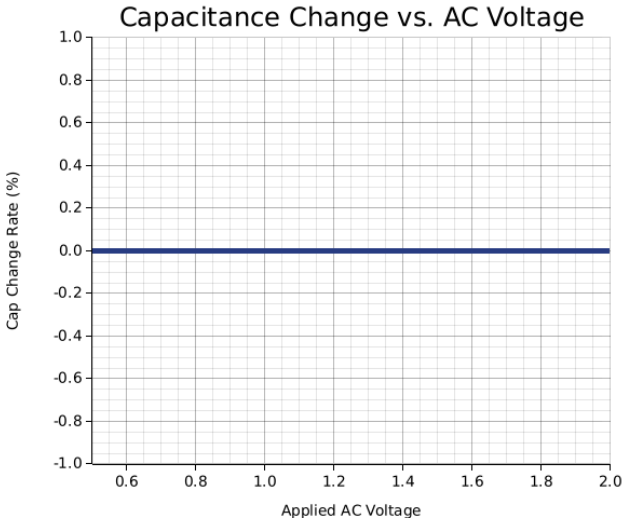



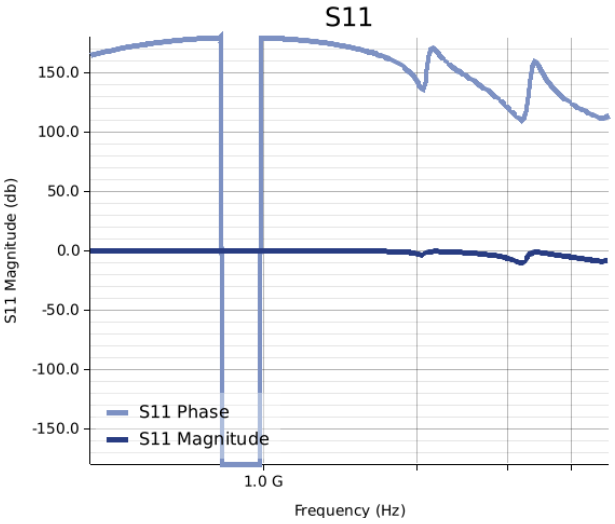


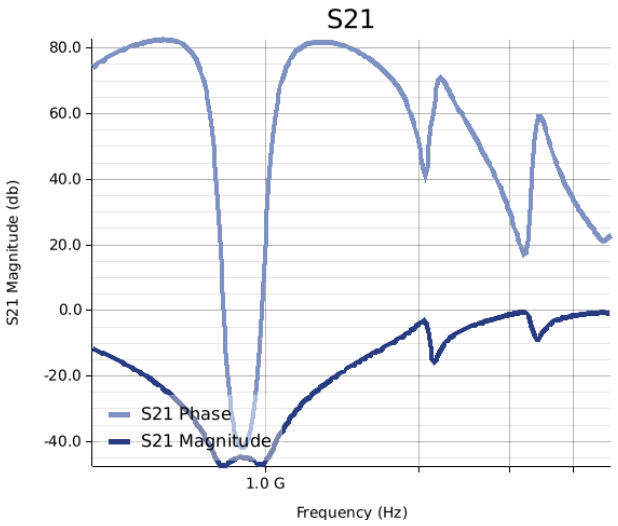

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**These are simulations.**
This is not a specification!

The responses shown represent the typical response for each part type. Specific responses may vary, depending on manufacturing variation affects of all parameters involved, including the specified tolerances applied to capacitance and unspecified variations of ESR, ESL, and leakage resistance.

The responses shown do not represent a specified or implied maximum capability of the device for all applications.

- The ESR used for ripple “Ripple Current/Voltage vs. Frequency” plots is the ESR at ambient temperature.
- The ESR in the “Temperature Rise vs. Ripple Current” plots is adjusted to each incremental temperature rise before the power and ripple current is calculated.
- The effects shown herein are based on measured data from a multiple part sample of the parts in question.
- Ripple capability of this device will be factored by thermal resistance (Rth) created by circuit traces (addi affects of all parameters involved, including the specified tolerances applied to capacitance and unspecified variations of ESR, ESL, and leakage resistance.
- The peak voltages generated in the “Temperature Rise vs. Combined Ripple Currents” plot are calculated for each frequency and are not combined with voltages generated at any other harmonics.
- Please consult with the catalog or field applications engineer for maximum capability of the device in specific applications.

All product information and data (collectively, the “Information”) are subject to change without notice.

KEMET K-SIM is designed to simulate behavior of components with respect to frequency, ambient temperature, and DC bias levels. The responses shown represent the typical response for each part type. Specific responses may vary, depending on manufacturing variation effects of all parameters involved, including the specified tolerances applied to capacitance and unspecified variations of ESR, ESL, and leakage resistance.

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If you have any questions please contact K-SIM.



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