Innovative Service Around the Globe YAGEO

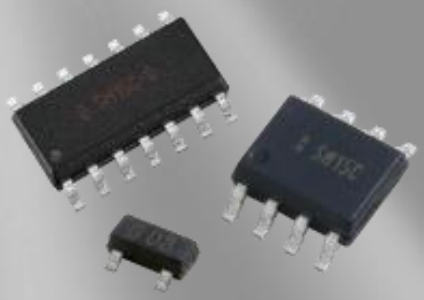
DATA SHEET

ELECTROSTATIC DISCHARGE PROTECTION DEVICES

INDUSTRIAL / CONSUMER

UBQ10A03L04-IR0.1

RoHS compliant & Halogen free



Product specification– March 14, 2023 V.0

Electrostatic Discharged Protection Devices (ESD) Data Sheet

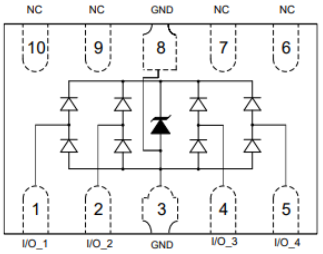
Features

- Transient protection for high-speed data lines
  IEC 61000-4-2 (ESD) ±15kV (Air) ±15kV (Contact)
  IEC 61000-4-5 (EFT) 5.0A (8/20us)
- Cable Discharge Event (CDE)
- Array of surge rated diodes with internal TVS diode
- Small package saves board space
- Protects four I/O lines
- Low capacitance: 0.70pF@0V(Typical)(I/O-GND)
  0.35pF@0V(Typical)(I/O-I/O)
- Low leakage current: 0.1μA @ VRWM (Maximum)
- Low clamping voltage
- Each I/O pin can withstand over 1000 ESD strikes for ±8kV contact discharge
- ROHS compliant
- Marking: B 34

Contact : 15KV
Air : 15KV

Applications

- HDMI 1.4/2.0, USB 3.0, MDDI, SATA ports
- Monitors and flat panel displays
- Set-top box
- Video graphics cards
- Digital Video Interface (DVI)
- Notebook computers

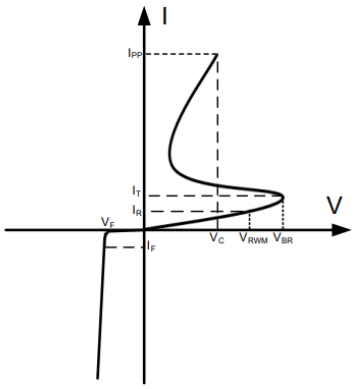


Pin Configuration

Maximum Ratings

Rating	Symbol	Value	Unit
Peak Pulse Power (8/20μs)	P_{PK}	20	W
ESD voltage (Contact discharge)	V_{ESD}	±15	KV
ESD voltage (Air discharge)		±15	
operating temperature range	T_{STG}	-55~+125	℃
Storage temperature	T_J	-55~+150	℃

Electrical Characteristics (T_J=25℃)

Symbol	Parameter	Diagram
V_{RWM}	Nominal Reverse Working Voltage	
I_R	Reverse Leakage Current @ VRWM	
V_{BR}	Reverse Breakdown Voltage @ IT	
I_T	Test Current for Reverse Breakdown	
V_H	Holding Voltage @I_T	
V_C	Clamping Voltage @ IPP	
I_{PP}	Maximum Peak Pulse Current	
C_{ESD}	Forward Current	
I_F	Forward Voltage @ IF	
V_F	Forward Voltage @ IF	

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Reverse stand-off voltage	V_{RWM}				3.3	V
Reverse breakdown voltage	V_{BR}	I_{BR}=1mA Between I/O and GND	5.0			V
Holding Voltage	V_H	I_T = 70mA Between I/O and GND		1.8		V
Reverse leakage current	I_R	V_R=3.3V Between I/O and GND			0.1	μA
Clamping voltage (tp=8/20μs)	V_C	I_{PP}=5A Between I/O and GND		8.0		V
Peak Pulse Current(tp=8/20μs)	I_{PP}				5	A
Clamping voltage	V_C	I_{PP}= 8.0A, tp=100ns(1)		3.50		V
		I_{PP}= 6.0A, tp=100ns(1)		5.20		V
Off state junction capacitance	C_J	0Vdc,f=1MHz Between I/O and GND		0.70		pF
Off state junction capacitance	C_J	VR = 0V, f = 1MHz Between I/O and I/O		0.35		pF

Notes:(1)Measurements performed using a 100ns Transmission Line Pulse(TLP) system between I/O and GND.

Typical Characteristics Curves

Figure 1. TLP Measurement of I/O to GND

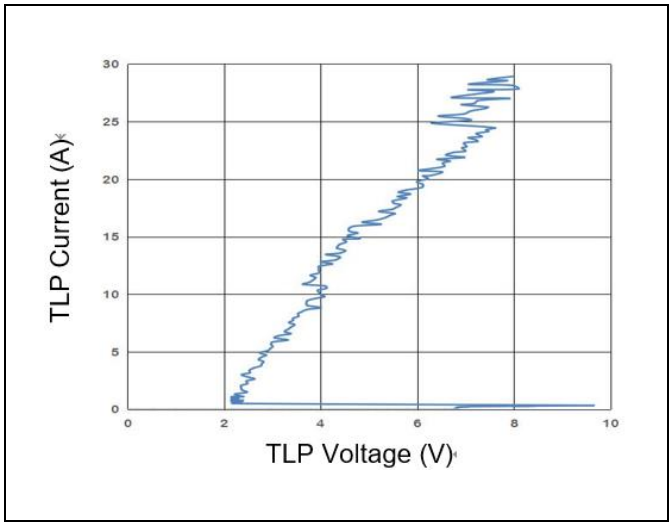


Figure 2. TLP Measurement of I/O to I/O

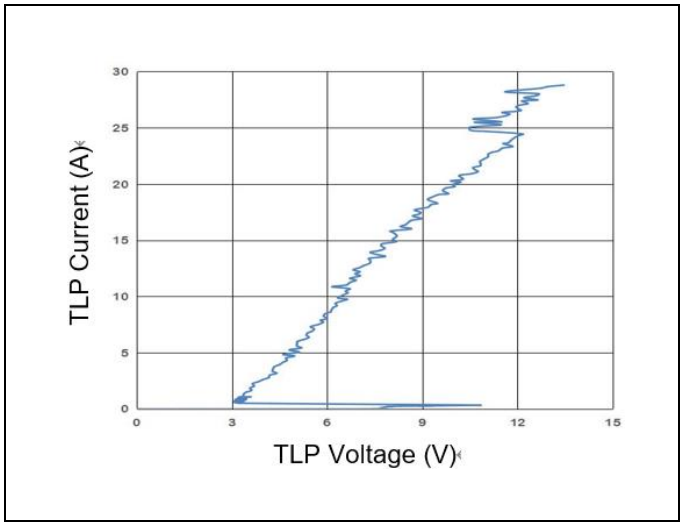


Figure 3. Capacitance vs Reverse Voltage IO to GND

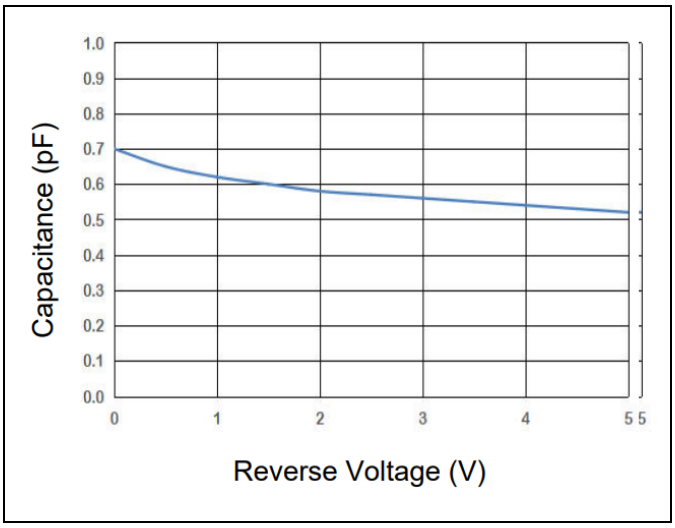
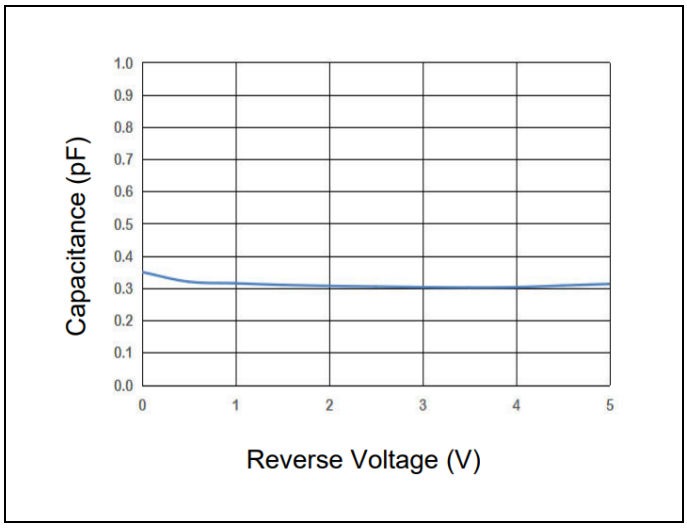
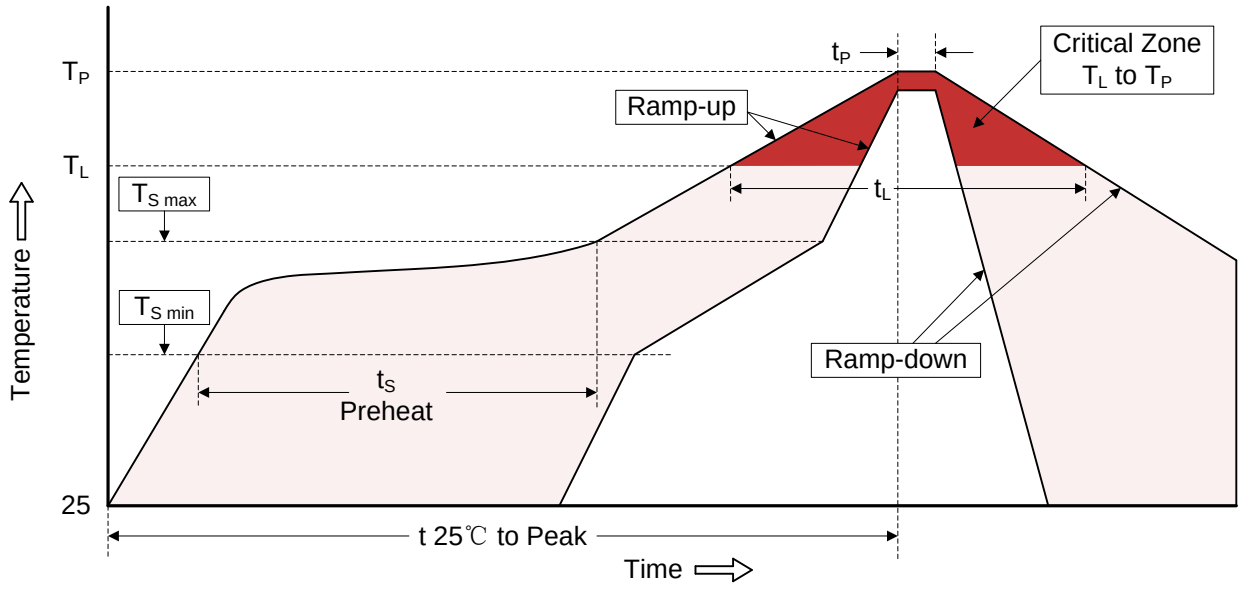


Figure 4. Capacitance vs Reverse Voltage IO to IO



Recommended Soldering Conditions

Reflow Soldering



Recommended Conditions

Profile Feature	Pb-Free Assembly
Average ramp-up rate (T_L to T_P)	3℃/second max.
Preheat -Temperature Min ($T_{S\ min}$) -Temperature Max ($T_{S\ max}$) -Time (min to max) (ts)	 150℃ 200℃ 60-180 seconds
$T_{S\ max}$ to T_L -Ramp-up Rate	3℃/second max.
Time maintained above: -Temperature (T_L) -Time (t_L)	 217℃ 60-150 seconds
Peak Temperature (T_P)	260℃
Time within 5℃ of actual Peak Temperature (t_P)	20-40 seconds
Ramp-down Rate	6℃/second max.
Time 25℃ to Peak Temperature	8 minutes max.

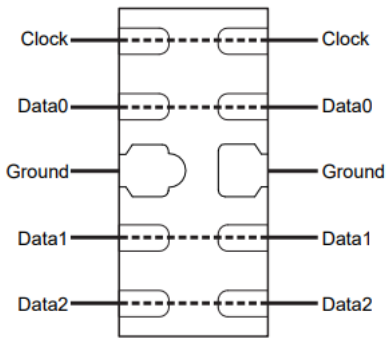
High Speed PCB Layout Guidelines

Printed circuit board layout is the key to achieving the highest level of surge immunity on power and data lines. The location of the protection devices on the PCB is the simplest and most important design rule to follow. The UBQ10A03L04-IR0.1 devices should be located as close as possible to the noise source.

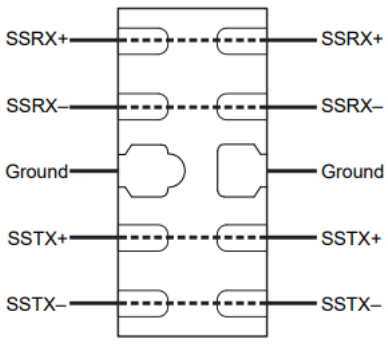
The UBQ10A03L04-IR0.1 device should be placed on all data and power lines that enter or exit the PCB at the I/O connector. In most systems, surge pulses occur on data and power lines that enter the PCB through the I/O connector. Placing the UBQ10A03L04-IR0.1 devices as close as possible to the noise source ensures that a surge voltage will be clamped before the pulse can be coupled into adjacent PCB traces. In addition, the PCB should use the shortest possible traces. A short trace length equates to low impedance, which ensures that the surge energy will be dissipated by the UBQ10A03L04-IR0.1 device. Long signal traces will act as antennas to receive energy from fields that are produced by the ESD pulse. By keeping line lengths as short as possible, the efficiency of the line to act as an antenna for ESD related fields is reduced. Minimize interconnecting line lengths by placing devices with the most interconnect as close together as possible.

The protection circuits should shunt the surge voltage to either the reference or chassis ground. Shunting the surge voltage directly to the IC's signal ground can cause ground bounce. The clamping performance of TVS diodes on a single ground PCB can be improved by minimizing the impedance with relatively short and wide ground traces. The PCB layout and IC package parasitic inductances can cause significant overshoot to the TVS's clamping voltage. The inductance of the PCB can be reduced by using short trace lengths and multiple layers with separate ground and power planes. One effective method to minimize loop problems is to incorporate a ground plane in the PCB design.

The UBQ10A03L04-IR0.1 ultra-low capacitance TVS is designed to protect four high speed data transmission lines from transient over-voltages by clamping them to a fixed reference. The low inductance and construction minimizes voltage overshoot during high current surges. When the voltage on the protected line exceeds the reference voltage the internal steering diodes are forward biased, conducting the transient current away from the sensitive circuitry. The UBQ10A03L04-IR0.1 is designed for ease of PCB layout by allowing the traces to run underneath the device. The pinout of the UBQ10A03L04-IR0.1 is designed to simply drop onto the IO lines of a High Definition Multimedia Interface (HDMI 1.4/2.0) or USB 3.0 design without having to divert the signal lines that may add more parasitic inductance. Pins 1, 2, 4 and 5 are connected to the internal TVS devices and pins 6, 7, 9 and 10 are no connects. The no connects was done so the package can be securely soldered onto the PCB surface.

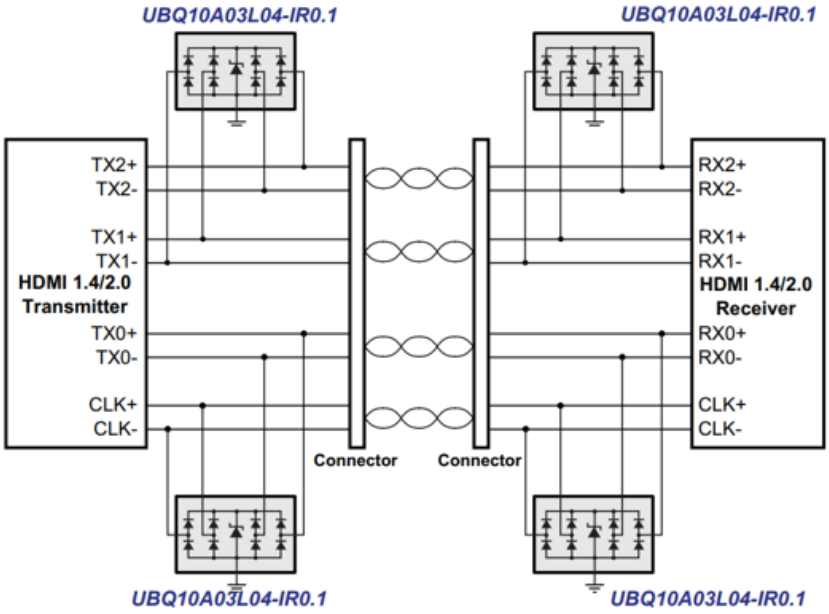


Flow Through Layout for HDMI 1.4/2.0

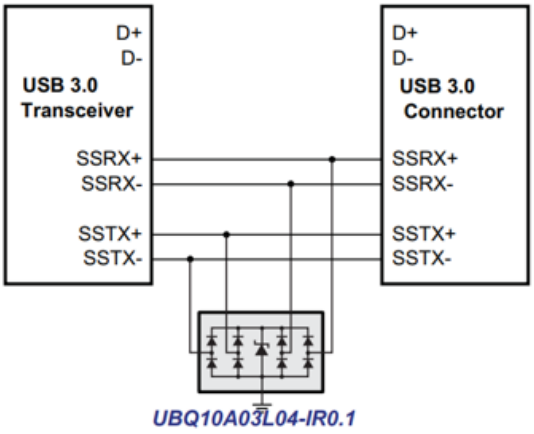


Flow Through Layout for USB 3.0

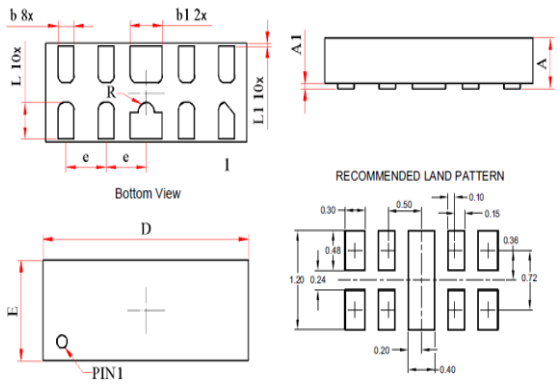
Application Information



HDMI 1.4/2.0 Ports



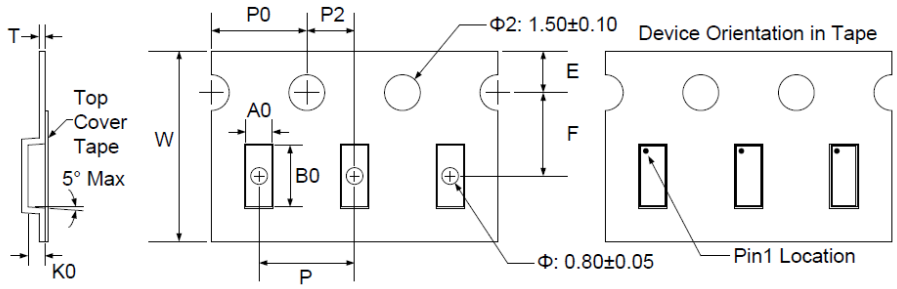
Dimensions (QFN-10L)



Symbol	Dimension					
	Millimeters			Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	0.450	--	0.550	0.018	--	0.026
A1	0.025	0.050	0.075	0.001	0.002	0.003
D	2.450	2.500	2.550	0.096	0.098	0.100
E	0.950	1.000	1.050	0.037	0.039	0.041
b	0.150	0.200	0.250	0.006	0.008	0.010
b1	0.350	0.400	0.450	0.014	0.016	0.018
L	0.320	0.370	0.420	0.013	0.015	0.017
L1	0.000	0.030	0.060	0.000	0.001	0.002
R	0.100 REF			0.004 REF		
e	0.500 BSC			0.020 BSC		

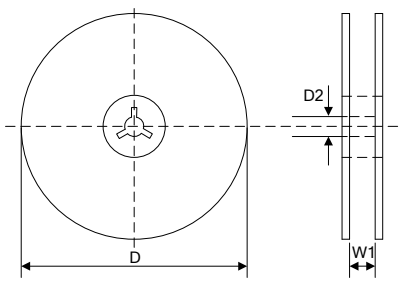
Packaging

Tape



Symbol	Dimension (mm)
W	8.00±0.30
A0	1.23±0.05
B0	2.70±0.05
K0	0.70±0.05
E	1.75±0.10
F	3.50±0.05
P	4.0±0.10
P0	4.0±0.10
P2	2.0±0.05
T	0.25±0.02

Reel



D	Φ178.0±2.0
D2	Φ13.0
W1	9.5
Quantity: 3000PCS	