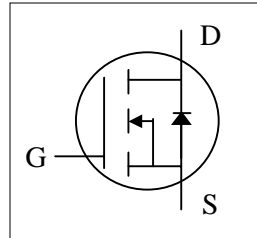
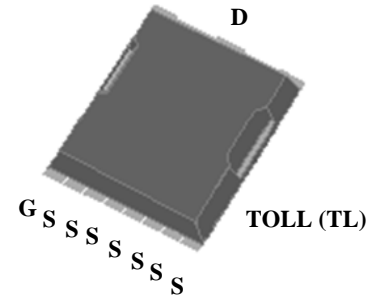


- ▼ 100% R_g & UIS Test
- ▼ Simple Drive Requirement
- ▼ Ultra Low On-resistance
- ▼ RoHS Compliant & Halogen-Free
- ▼ AEC Qualified



BV_{DSS}	100V
$R_{DS(ON)}$	1.5m Ω



Description

XP10NA1R5 series are innovated design and silicon process technology to achieve the lowest possible on-resistance and fast switching performance. It provides the designer with an extreme efficient device for use in a wide range of power applications.

The TOLL package is a perfect solution for high power density and high power efficiency application.

Absolute Maximum Ratings @T_j=25°C(unless otherwise specified)

Symbol	Parameter	Rating	Units
V _{DS}	Drain-Source Voltage	100	V
V _{GS}	Gate-Source Voltage	+20	V
I _D @T _C =25°C	Drain Current, V _{GS} @ 10V ⁴ (Silicon Limited)	347	A
I _D @T _C =25°C	Drain Current, V _{GS} @ 10V ⁴	300	A
I _D @T _C =100°C	Drain Current, V _{GS} @ 10V	245	A
I _{DM}	Pulsed Drain Current ¹	1200	A
P _D @T _C =25°C	Total Power Dissipation	333	W
P _D @T _A =25°C	Total Power Dissipation ³	3.75	W
E _{AS}	Single Pulse Avalanche Energy ⁵	500	mJ
T _{STG}	Storage Temperature Range	-55 to 175	°C
T _J	Operating Junction Temperature Range	-55 to 175	°C

Thermal Data

Symbol	Parameter	Value	Units
R _{thj-c}	Maximum Thermal Resistance, Junction-case	0.45	°C/W
R _{thj-a}	Maximum Thermal Resistance, Junction-ambient (PCB mount) ³	40	°C/W

Electrical Characteristics @ $T_j=25^{\circ}\text{C}$ (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	100	-	-	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance ²	$V_{GS}=10V, I_D=100A$	-	-	1.5	m Ω
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	2	-	4	V
g_{fs}	Forward Transconductance	$V_{DS}=5V, I_D=100A$	-	195	-	S
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=80V, V_{GS}=0V$	-	-	25	μA
I_{GSS}	Gate-Source Leakage	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 0.1	μA
Q_g	Total Gate Charge ⁶	$I_D=100A$	-	205	328	nC
Q_{gs}	Gate-Source Charge ⁶	$V_{DS}=50V$	-	50	-	nC
Q_{gd}	Gate-Drain ("Miller") Charge ⁶	$V_{GS}=10V$	-	72	-	nC
$t_{d(on)}$	Turn-on Delay Time ⁶	$V_{DS}=50V$	-	37	-	ns
t_r	Rise Time ⁶	$I_D=100A$	-	168	-	ns
$t_{d(off)}$	Turn-off Delay Time ⁶	$R_G=5.1\Omega$	-	105	-	ns
t_f	Fall Time ⁶	$V_{GS}=10V$	-	230	-	ns
C_{iss}	Input Capacitance ⁶	$V_{GS}=0V$	-	10450	16720	pF
C_{oss}	Output Capacitance ⁶	$V_{DS}=80V$	-	1550	-	pF
C_{rss}	Reverse Transfer Capacitance ⁶	$f=1.0\text{MHz}$	-	45	-	pF
R_g	Gate Resistance	$f=1.0\text{MHz}$	-	0.8	1.6	Ω

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{SD}	Forward On Voltage ²	$I_S=100A, V_{GS}=0V$	-	-	1.3	V
t_{rr}	Reverse Recovery Time ⁶	$I_S=100A, V_{GS}=0V$	-	135	-	ns
Q_{rr}	Reverse Recovery Charge ⁶	$dI/dt=100A/\mu s$	-	300	-	nC

Notes:

1. Pulse width limited by Max. junction temperature.
2. Pulse test
3. Surface mounted on 1 in² copper pad of FR4 board
4. Package limitation current is 300A .
5. Starting $T_j=25^{\circ}\text{C}$, $V_{DD}=50V$, $L=0.1\text{mH}$, $R_G=25\Omega$, $V_{GS}=10V$
6. Defined by design. Not subject to production test.

THIS PRODUCT IS SENSITIVE TO ELECTROSTATIC DISCHARGE, PLEASE HANDLE WITH CAUTION.

USE OF THIS PRODUCT AS A CRITICAL COMPONENT IN LIFE SUPPORT OR OTHER SIMILAR SYSTEMS IS NOT AUTHORIZED.

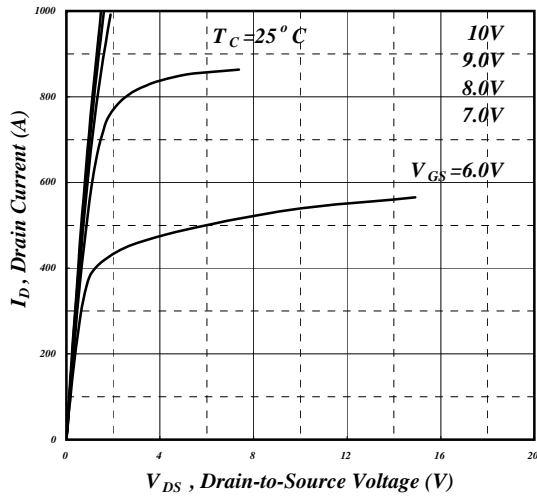


Fig 1. Typical Output Characteristics

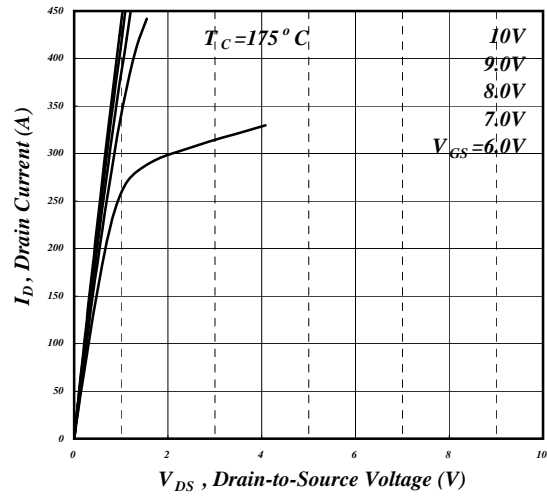


Fig 2. Typical Output Characteristics

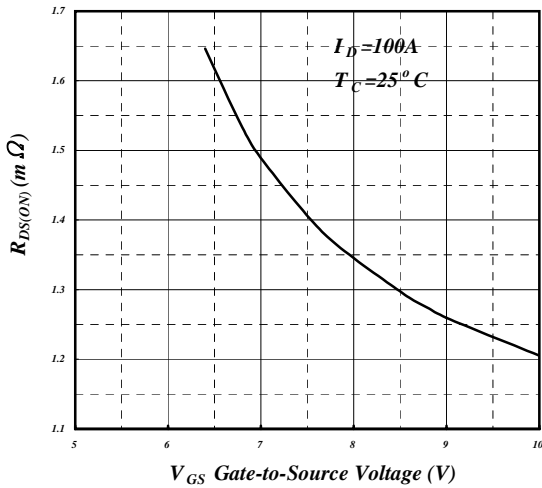


Fig 3. On-Resistance v.s. Gate Voltage

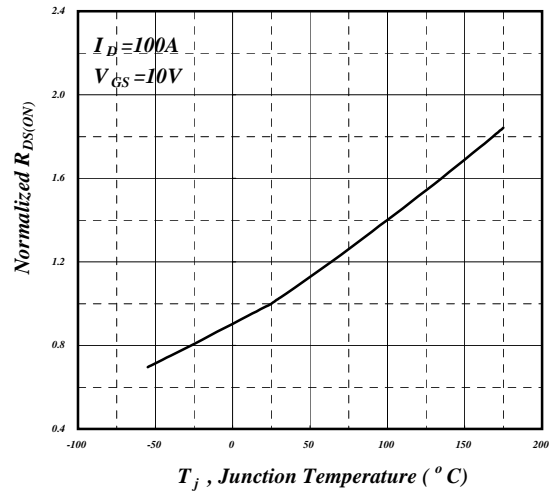


Fig 4. Normalized On-Resistance v.s. Junction Temperature

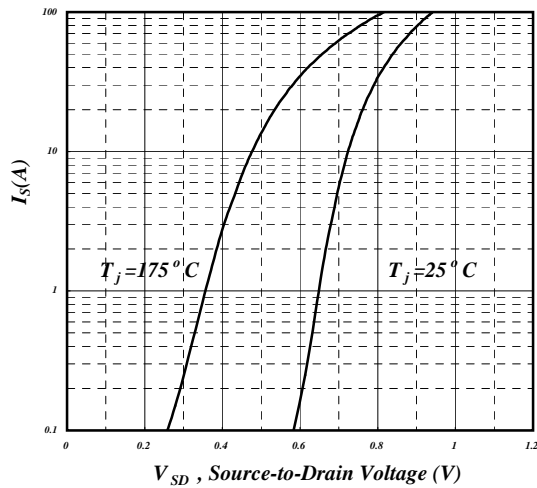


Fig 5. Forward Characteristic of Reverse Diode

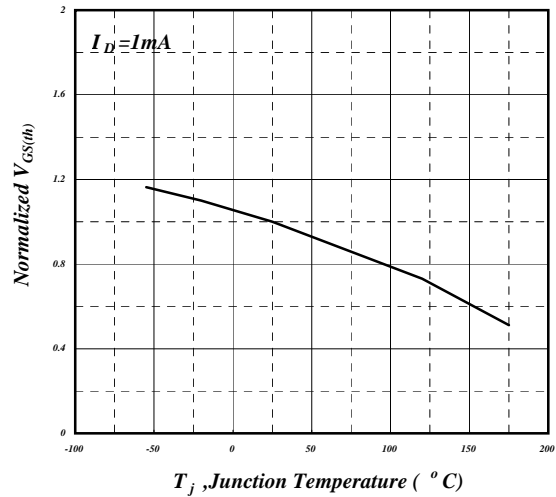


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

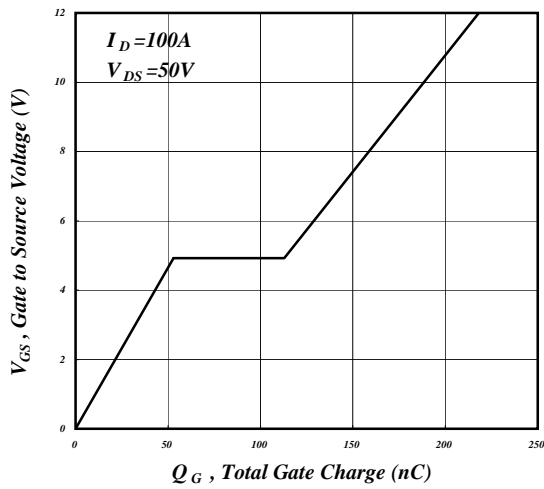


Fig 7. Gate Charge Characteristics

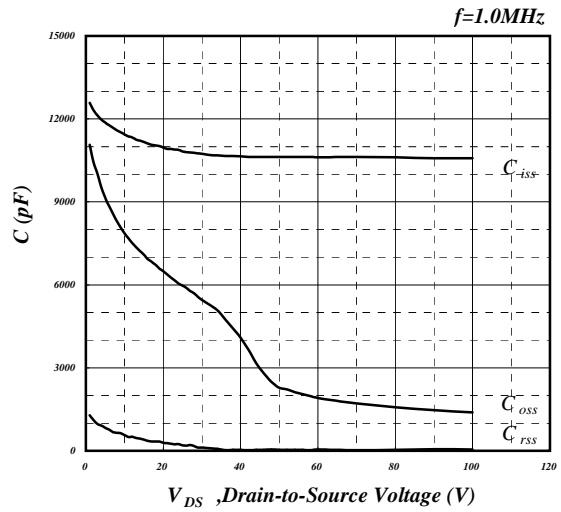


Fig 8. Typical Capacitance Characteristics

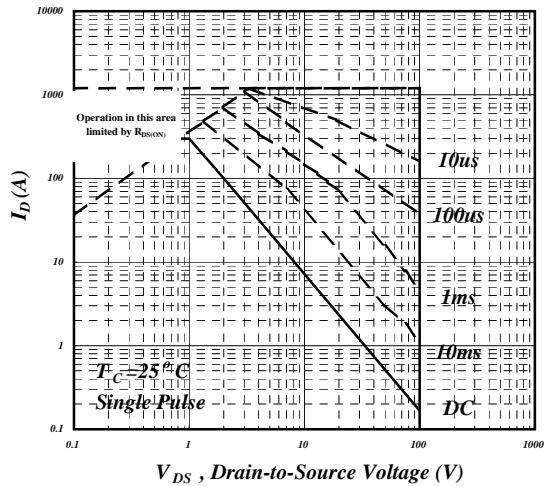


Fig 9. Maximum Safe Operating Area

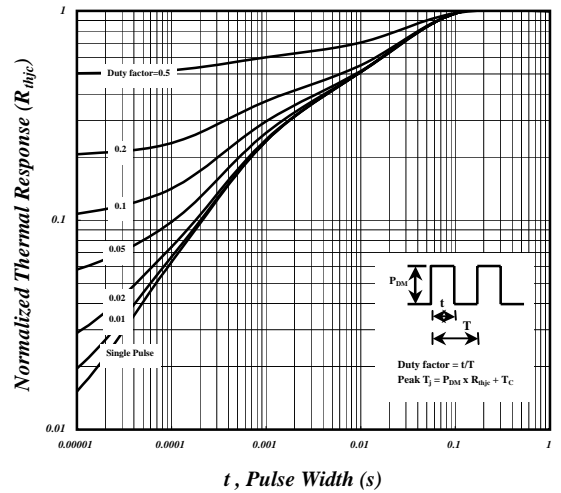


Fig 10. Effective Transient Thermal Impedance

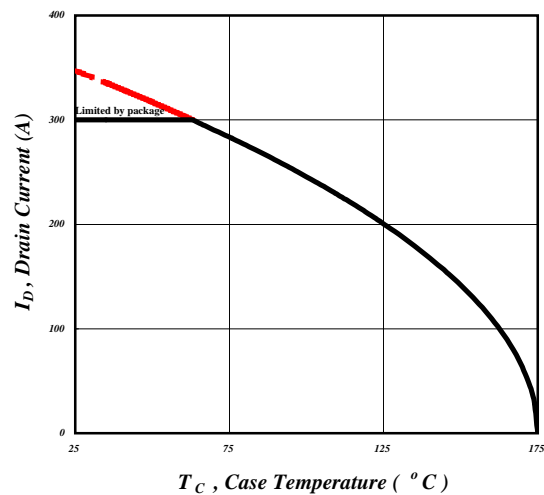


Fig 11. Drain Current v.s. Case Temperature

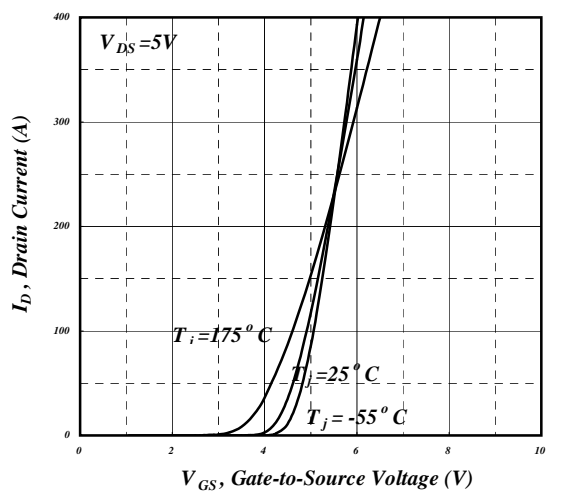


Fig 12. Transfer Characteristics

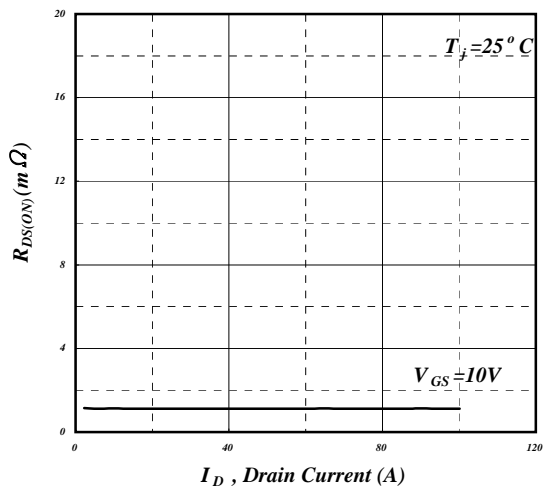


Fig 13. Typ. Drain-Source on State Resistance

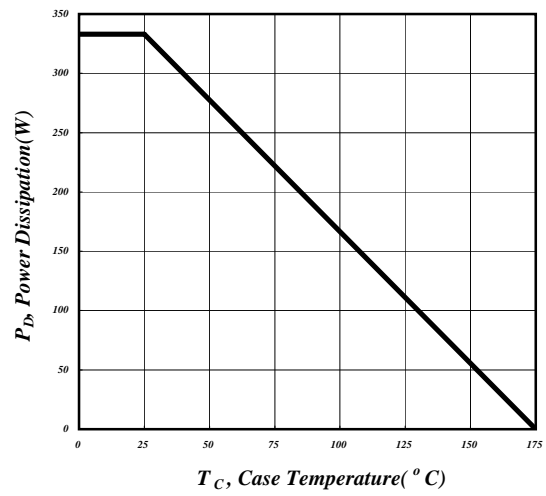
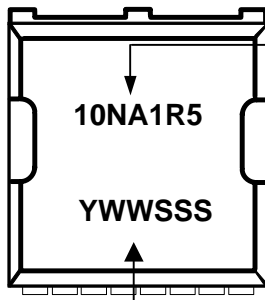


Fig 14. Total Power Dissipation

MARKING INFORMATION



Part Number

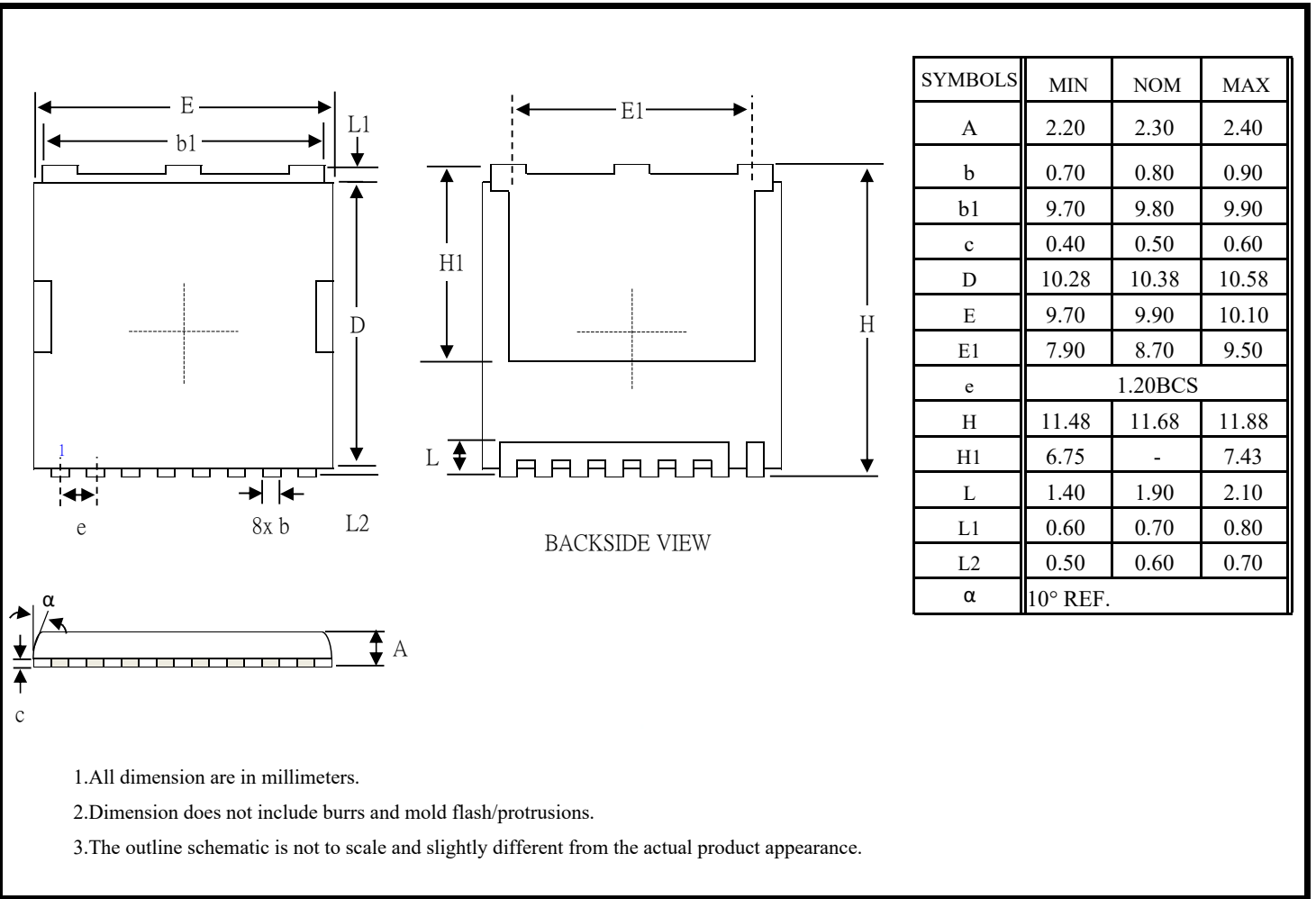
Date Code (YWWSSS)

Y : Last Digit Of The Year

WW : Week

SSS : Sequence

Package Outline : TOLL



- 1.All dimension are in millimeters.
- 2.Dimension does not include burrs and mold flash/protrusions.
- 3.The outline schematic is not to scale and slightly different from the actual product appearance.

TOLL FOOTPRINT :

