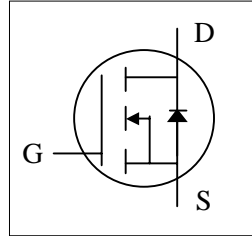
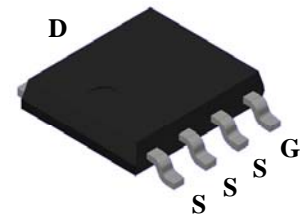


- ▼ 100% R_g & UIS Test
- ▼ Simple Drive Requirement
- ▼ Low On-resistance
- ▼ RoHS Compliant & Halogen-Free



BV _{DSS}	40V
R _{DS(ON)}	2.28mΩ



SPPAK 5x6

Description

AP4NA2R2HC series are innovated design and silicon process technology to achieve the lowest possible on-resistance and fast switching performance. It provides the designer with an extreme efficient device for use in a wide range of power applications.

The SPPAK 5x6 package is special for DC-DC converters application and the foot print is compatible with SO-8 with backside heat sink and lower profile.

Absolute Maximum Ratings @T_j=25°C (unless otherwise specified)

Symbol	Parameter	Rating	Units
V _{DS}	Drain-Source Voltage	40	V
V _{GS}	Gate-Source Voltage	±20	V
I _D @T _C =25°C	Drain Current, V _{GS} @ 10V ⁵ (Silicon Limited)	160	A
I _D @T _C =25°C	Drain Current, V _{GS} @ 10V ⁵ (Package Limited)	100	A
I _D @T _C =100°C	Drain Current, V _{GS} @ 10V ⁵ (Package Limited)	100	A
I _D @T _A =25°C	Drain Current, V _{GS} @ 10V ³	36.5	A
I _D @T _A =70°C	Drain Current, V _{GS} @ 10V ³	29	A
I _{DM}	Pulsed Drain Current ¹	500	A
P _D @T _C =25°C	Total Power Dissipation	96.1	W
P _D @T _A =25°C	Total Power Dissipation ³	5	W
E _{AS}	Single Pulse Avalanche Energy ⁴	80	mJ
T _{STG}	Storage Temperature Range	-55 to 150	°C
T _J	Operating Junction Temperature Range	-55 to 150	°C

Thermal Data

Symbol	Parameter	Value	Unit
R _{thj-c}	Maximum Thermal Resistance, Junction-case	1.3	°C/W
R _{thj-a}	Maximum Thermal Resistance, Junction-ambient ³	25	°C/W

Electrical Characteristics @ $T_j=25^{\circ}\text{C}$ (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	40	-	-	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance ²	$V_{GS}=10V, I_D=40A$	-	-	2.28	$m\Omega$
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	2	-	4	V
g_{fs}	Forward Transconductance	$V_{DS}=5V, I_D=40A$	-	120	-	S
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=32V, V_{GS}=0V$	-	-	10	μA
I_{GSS}	Gate-Source Leakage	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 0.1	μA
Q_g	Total Gate Charge ⁶	$I_D=40A$	-	50	80	nC
Q_{gs}	Gate-Source Charge ⁶	$V_{DS}=20V$	-	12	-	nC
Q_{gd}	Gate-Drain ("Miller") Charge ⁶	$V_{GS}=10V$	-	14	-	nC
$t_{d(on)}$	Turn-on Delay Time ⁶	$V_{DS}=20V$	-	12	-	ns
t_r	Rise Time ⁶	$I_D=40A$	-	72	-	ns
$t_{d(off)}$	Turn-off Delay Time ⁶	$R_G=3.3\Omega$	-	34	-	ns
t_f	Fall Time ⁶	$V_{GS}=10V$	-	12	-	ns
C_{iss}	Input Capacitance ⁶	$V_{GS}=0V$	-	2500	4000	pF
C_{oss}	Output Capacitance ⁶	$V_{DS}=30V$	-	570	-	pF
C_{rss}	Reverse Transfer Capacitance ⁶	$f=1.0\text{MHz}$	-	50	-	pF
R_g	Gate Resistance	$f=1.0\text{MHz}$	-	1.5	3	Ω

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{SD}	Forward On Voltage ²	$I_S=40A, V_{GS}=0V$	-	-	1.2	V
t_{rr}	Reverse Recovery Time ⁶	$I_S=40A, V_{GS}=0V,$	-	33	-	ns
Q_{rr}	Reverse Recovery Charge ⁶	$di/dt=100A/\mu s$	-	22	-	nC

Notes:

1. Pulse width limited by Max. junction temperature.
2. Pulse test
3. Surface mounted on 1 in² copper pad of FR4 board, $t \leq 10\text{sec}$; 60°C/W at steady state.
4. Starting $T_j=25^{\circ}\text{C}$, $V_{DD}=30V$, $L=0.1\text{mH}$, $R_G=25\Omega$, $V_{GS}=10V$
5. Package limitation current is 100A.
6. Guaranteed by design.
7. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{j(MAX)}=150^{\circ}\text{C}$.

THIS PRODUCT IS SENSITIVE TO ELECTROSTATIC DISCHARGE, PLEASE HANDLE WITH CAUTION.

USE OF THIS PRODUCT AS A CRITICAL COMPONENT IN LIFE SUPPORT, AUTOMOTIVE OR OTHER SIMILAR SYSTEMS IS NOT AUTHORIZED.

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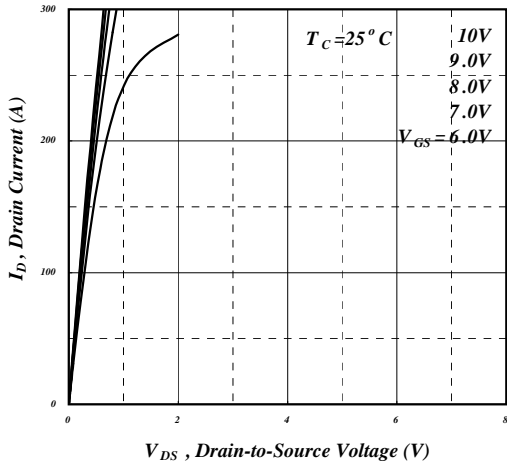


Fig 1. Typical Output Characteristics

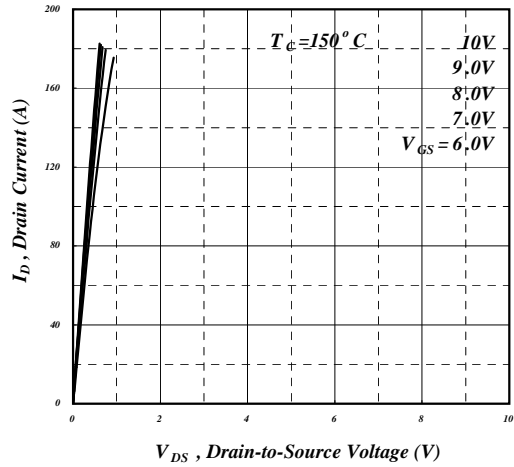


Fig 2. Typical Output Characteristics

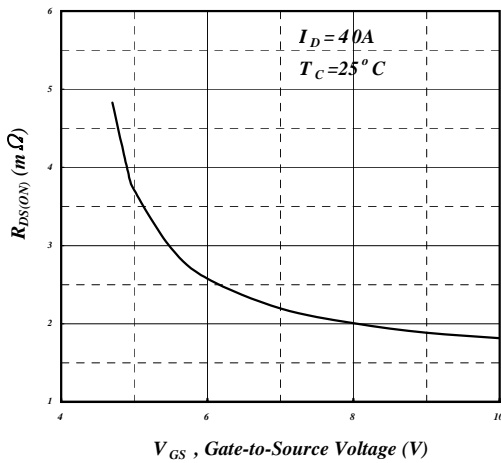


Fig 3. On-Resistance v.s. Gate Voltage

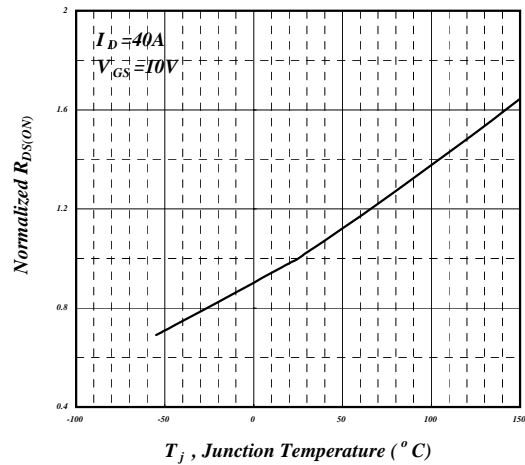


Fig 4. Normalized On-Resistance v.s. Junction Temperature

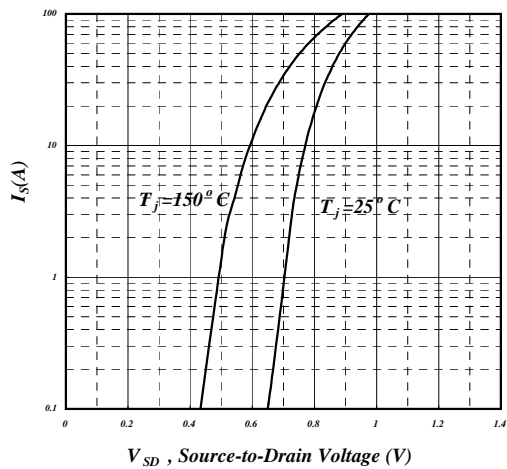


Fig 5. Forward Characteristic of Reverse Diode

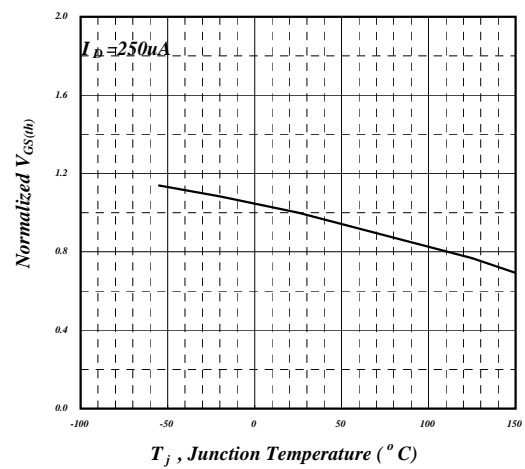


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

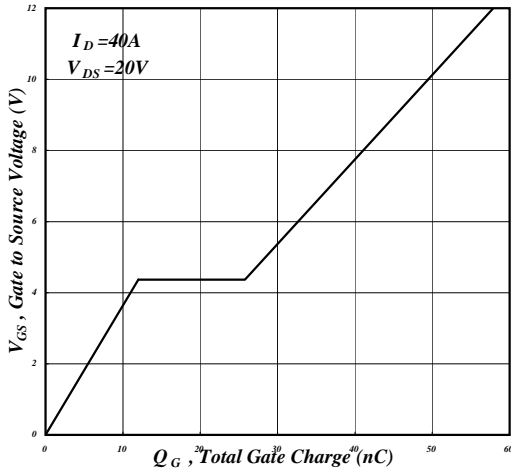


Fig 7. Gate Charge Characteristics

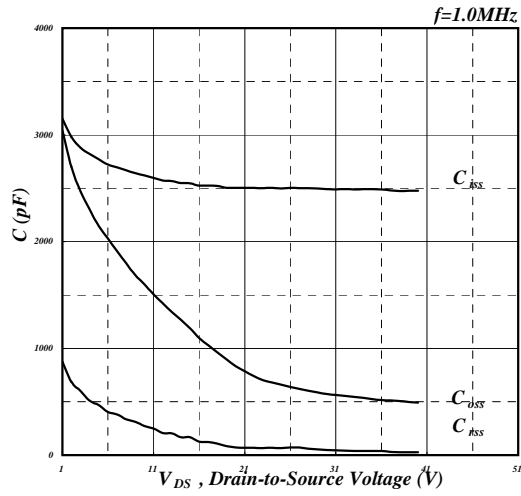


Fig 8. Typical Capacitance Characteristics

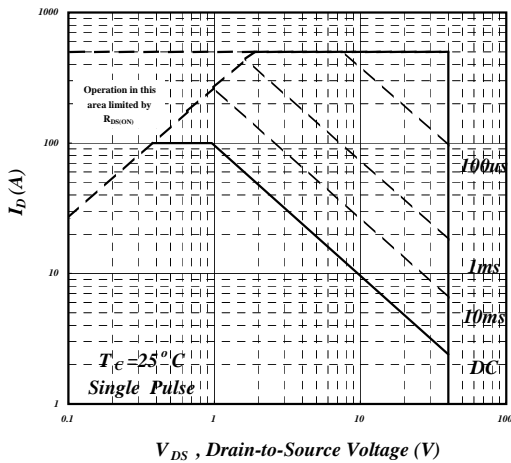


Fig 9. Maximum Safe Operating Area⁷

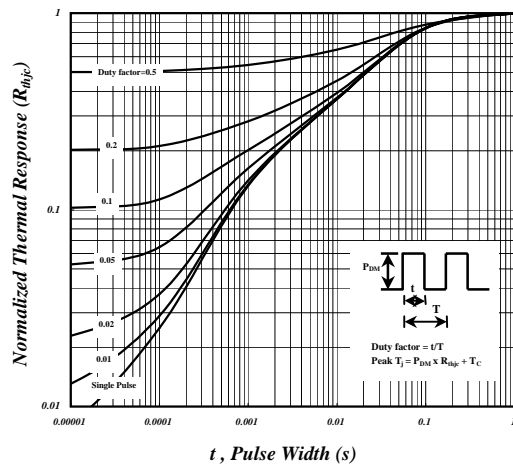


Fig 10. Effective Transient Thermal Impedance

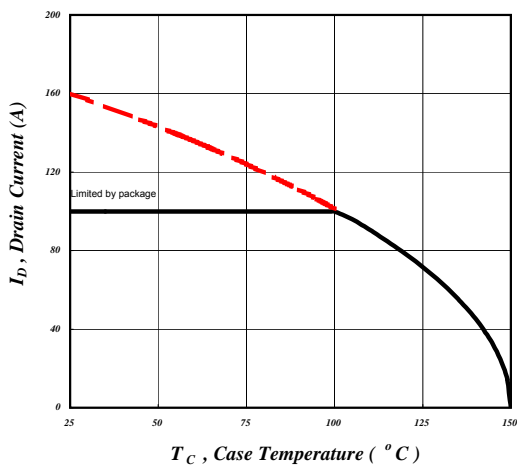


Fig 11. Drain Current v.s. Case Temperature

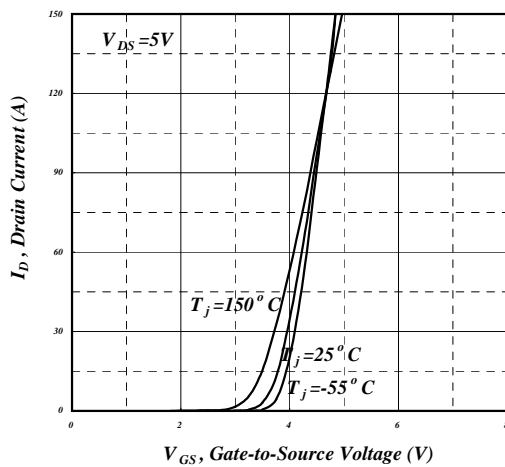


Fig 12. Transfer Characteristics

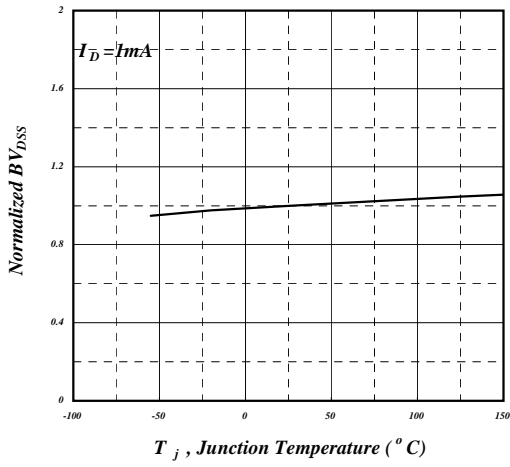


Fig 13. Normalized BV_{DSS} v.s. Junction Temperature

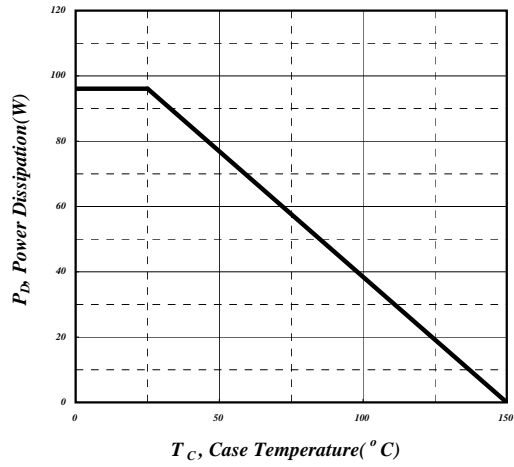


Fig 14. Total Power Dissipation

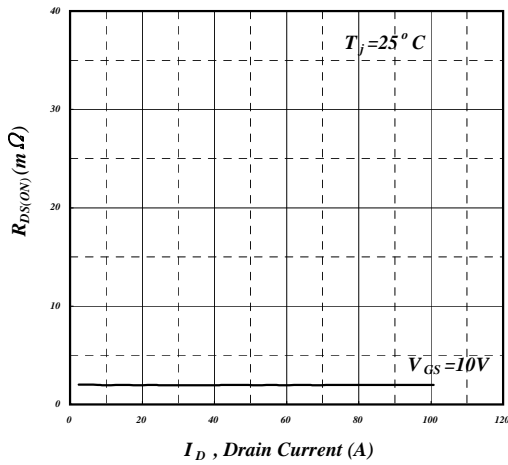
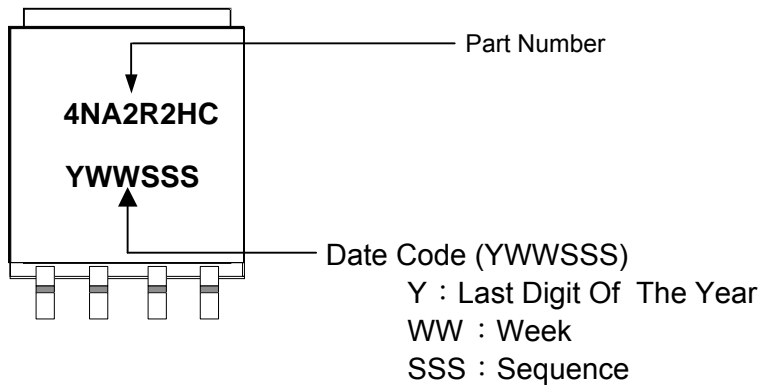
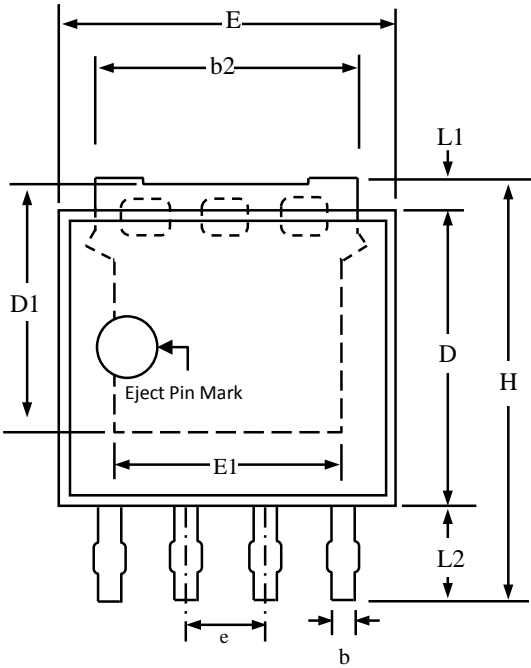


Fig 15. Typ. Drain-Source on State Resistance

MARKING INFORMATION

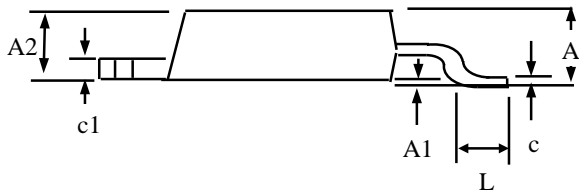


Package Outline : SPPAK 5X6



SYMBOLS	Millimeters		
	MIN	NOM	MAX
A	1.00	-	1.30
A1	0	0.075	0.15
A2	0.98	1.05	1.12
b	0.35	0.42	0.50
b2	4.02	4.23	4.41
c	0.19	0.22	0.25
c1	0.24	0.27	0.30
D	4.45	-	4.70
D1	-	-	4.45
E	4.95	-	5.30
E1	3.50	-	3.70
e	1.27 BSC		
H	5.95	-	6.25
L	0.40	-	0.85
L1	0.27	-	0.57
L2	0.80	-	1.30

- 1.All Dimensions Are in Millimeters.
- 2.Dimension Does Not Include Mold Protrusions.



SPPAK 5X6 FOOTPRINT :

