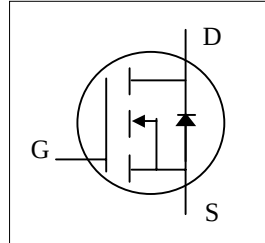
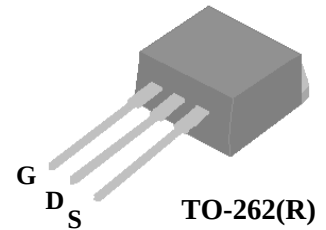


- ▼ 100% R_g & UIS Test
- ▼ Low t_{rr} / Q_{rr}
- ▼ Simple Drive Requirement
- ▼ RoHS Compliant & Halogen-Free



BV_{DSS}	600V
$R_{DS(ON)}$	0.12 Ω
$I_D^{3,4}$	27A



Description

XP60SC120D series are innovated design and silicon process technology to achieve the lowest possible on-resistance and fast switching performance. It provides the designer with an extreme efficient device for use in a wide range of power applications.

The TO-262 package is widely preferred for commercial-industrial through-hole applications and suited for low voltage applications such as DC/DC converters.

Absolute Maximum Ratings@ $T_j=25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	600	V
V_{GS}	Gate-Source Voltage	± 20	V
V_{GS}	Gate-Source Voltage, AC ($f > 1\text{Hz}$)	± 30	V
$I_D@T_C=25^\circ\text{C}$	Drain Current, $V_{GS} @ 10V^{3,4}$	27	A
$I_D@T_C=100^\circ\text{C}$	Drain Current, $V_{GS} @ 10V^{3,4}$	17	A
I_{DM}	Pulsed Drain Current ¹	72	A
dv/dt	MOSFET dv/dt Ruggedness ($V_{DS} = 0 \dots 480V$)	30	V/ns
$P_D@T_C=25^\circ\text{C}$	Total Power Dissipation	156	W
$P_D@T_A=25^\circ\text{C}$	Total Power Dissipation	2	W
E_{AS}	Single Pulse Avalanche Energy ⁵	200	mJ
dv/dt	Peak Diode Recovery dv/dt^6	15	V/ns
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ\text{C}$
T_j	Operating Junction Temperature Range	-55 to 150	$^\circ\text{C}$

Thermal Data

Symbol	Parameter	Value	Units
R_{thj-c}	Maximum Thermal Resistance, Junction-case	0.8	$^\circ\text{C}/\text{W}$
R_{thj-a}	Maximum Thermal Resistance, Junction-ambient	62	$^\circ\text{C}/\text{W}$

Electrical Characteristics@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =1mA	600	-	-	V
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =10V, I _D =8.6A	-	-	0.12	Ω
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250uA	2.5	-	4.5	V
g _{fs}	Forward Transconductance	V _{DS} =10V, I _D =8.6A	-	14	-	S
I _{DSS}	Drain-Source Leakage Current	V _{DS} =480V, V _{GS} =0V	-	-	100	uA
I _{GSS}	Gate-Source Leakage	V _{GS} =±20V, V _{DS} =0V	-	-	±1	uA
Q _g	Total Gate Charge	I _D =12A	-	52	83	nC
Q _{gs}	Gate-Source Charge	V _{DS} =480V	-	16	-	nC
Q _{gd}	Gate-Drain ("Miller") Charge	V _{GS} =10V	-	22.5	-	nC
t _{d(on)}	Turn-on Delay Time	V _{DD} =300V	-	19	-	ns
t _r	Rise Time	I _D =12A	-	39	-	ns
t _{d(off)}	Turn-off Delay Time	R _G =3.3Ω	-	60	-	ns
t _f	Fall Time	V _{GS} =10V	-	28	-	ns
C _{iss}	Input Capacitance	V _{GS} =0V	-	2150	3440	pF
C _{oss}	Output Capacitance	V _{DS} =100V	-	77	-	pF
C _{rss}	Reverse Transfer Capacitance	f=1.0MHz	-	10	-	pF
R _g	Gate Resistance	f=1.0MHz	-	6.25	12.5	Ω

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V _{SD}	Forward On Voltage ²	I _S =8.6A, V _{GS} =0V	-	0.85	1.5	V
t _{rr}	Reverse Recovery Time	I _S =12A, V _{GS} =0V	-	185	-	ns
Q _{rr}	Reverse Recovery Charge	di/dt=100A/μs	-	1.8	-	μC

Notes:

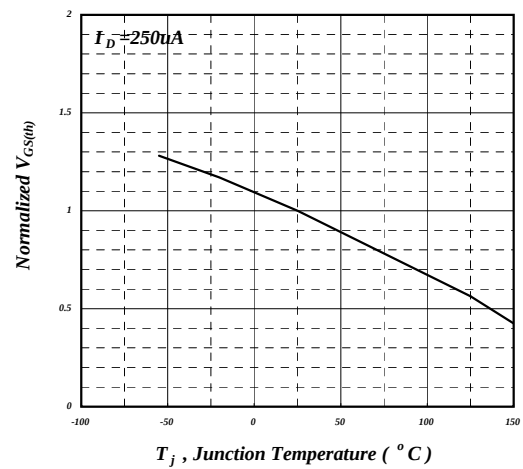
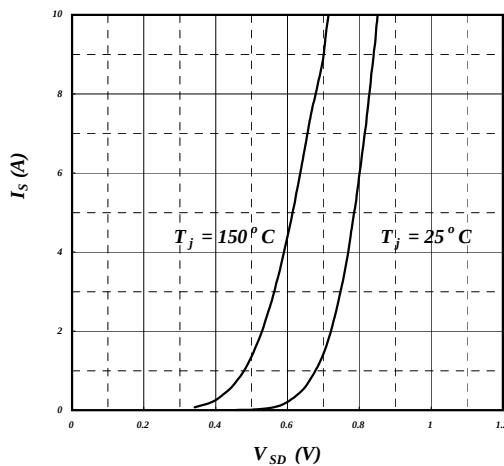
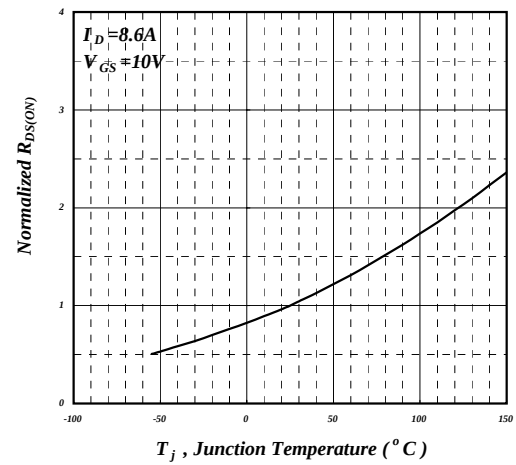
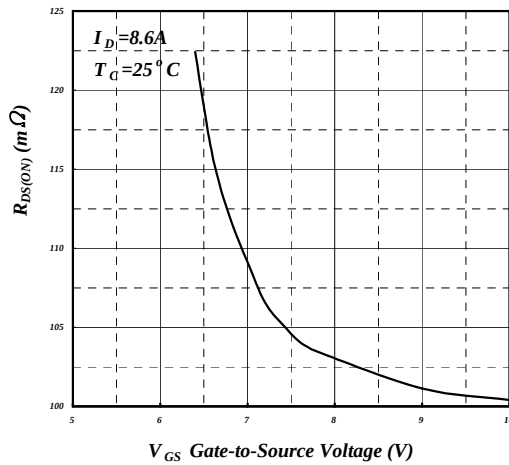
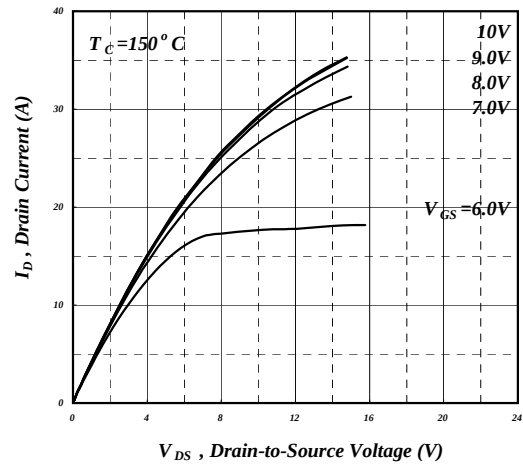
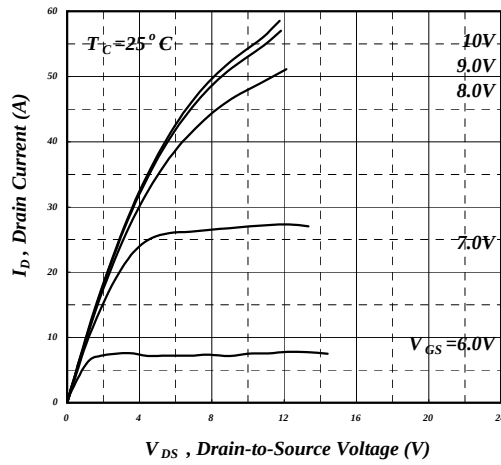
- 1.Pulse width limited by max. junction temperature.
- 2.Pulse test
- 3.Limited by max. junction temperature. Maximum duty cycle D=0.75
- 4.Ensure that the junction temperature does not exceed T_{jmax}.
- 5.Starting T_j=25°C, V_{DD}=90V, L=100mH, R_G=25Ω, V_{GS}=10V
- 6.I_{SD} ≤ I_D, V_{DD} ≤ BV_{DSS}, starting T_j = 25°C

THIS PRODUCT IS SENSITIVE TO ELECTROSTATIC DISCHARGE, PLEASE HANDLE WITH CAUTION.

USE OF THIS PRODUCT AS A CRITICAL COMPONENT IN LIFE SUPPORT, AUTOMOTIVE OR OTHER SIMILAR SYSTEMS IS NOT AUTHORIZED.

XSEMI DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

XSEMI RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN.



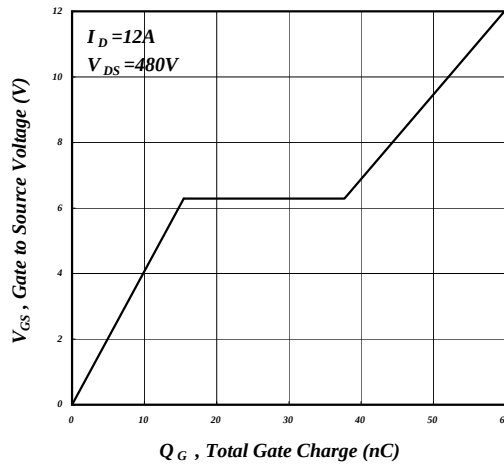


Fig 7. Gate Charge Characteristics

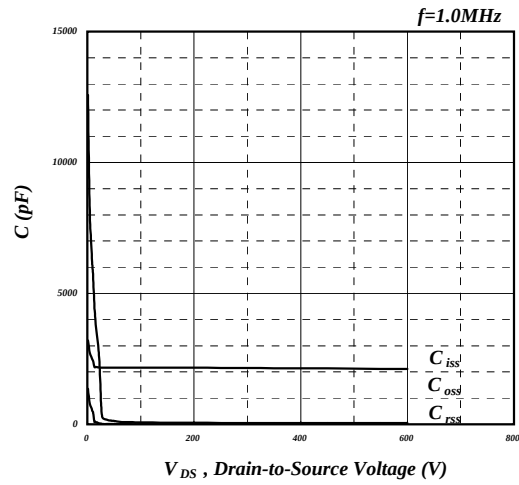


Fig 8. Typical Capacitance Characteristics

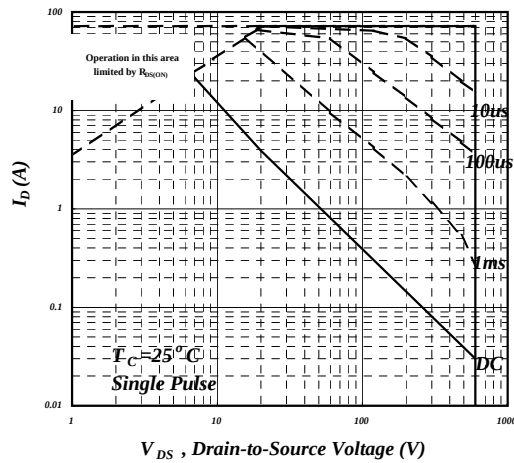


Fig 9. Maximum Safe Operating Area

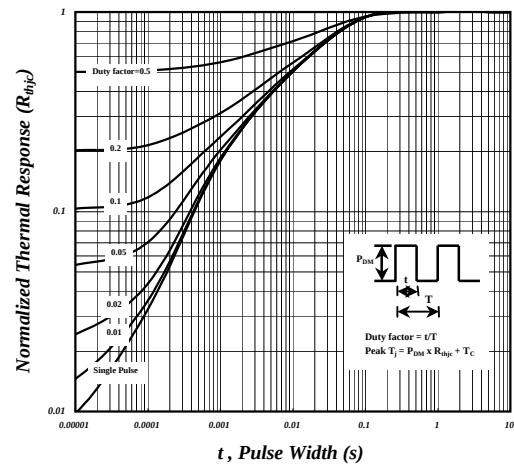


Fig10. Effective Transient Thermal Impedance

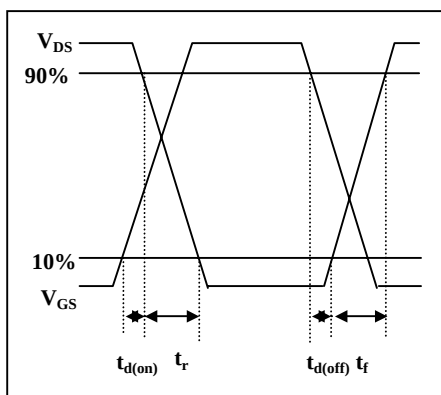


Fig 11. Switching Time Waveform

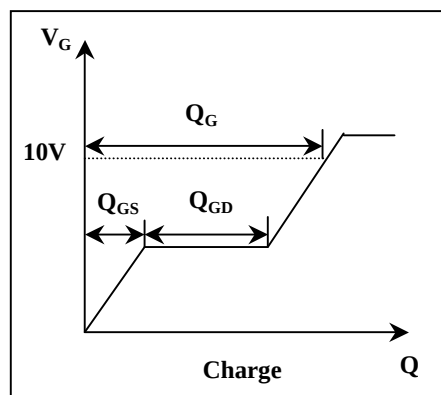


Fig 12. Gate Charge Waveform

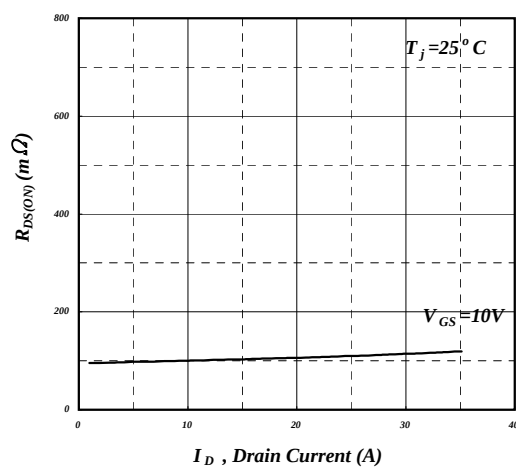


Fig 13. Typ. Drain-Source on State Resistance

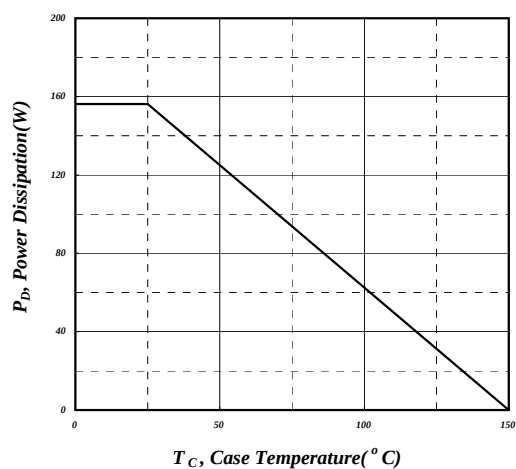
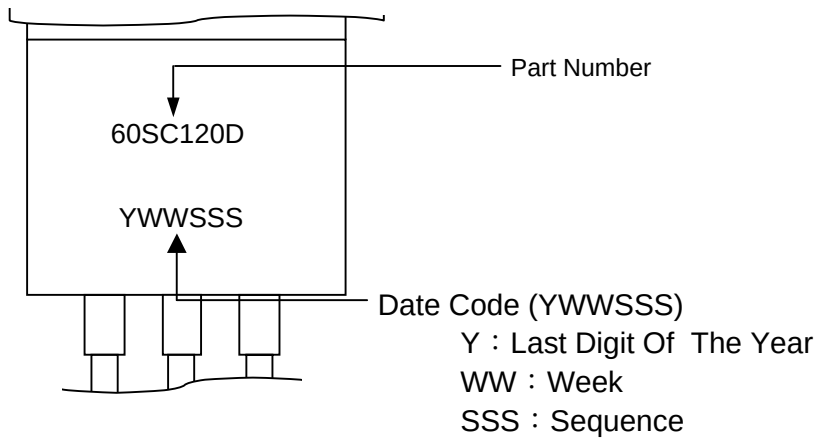
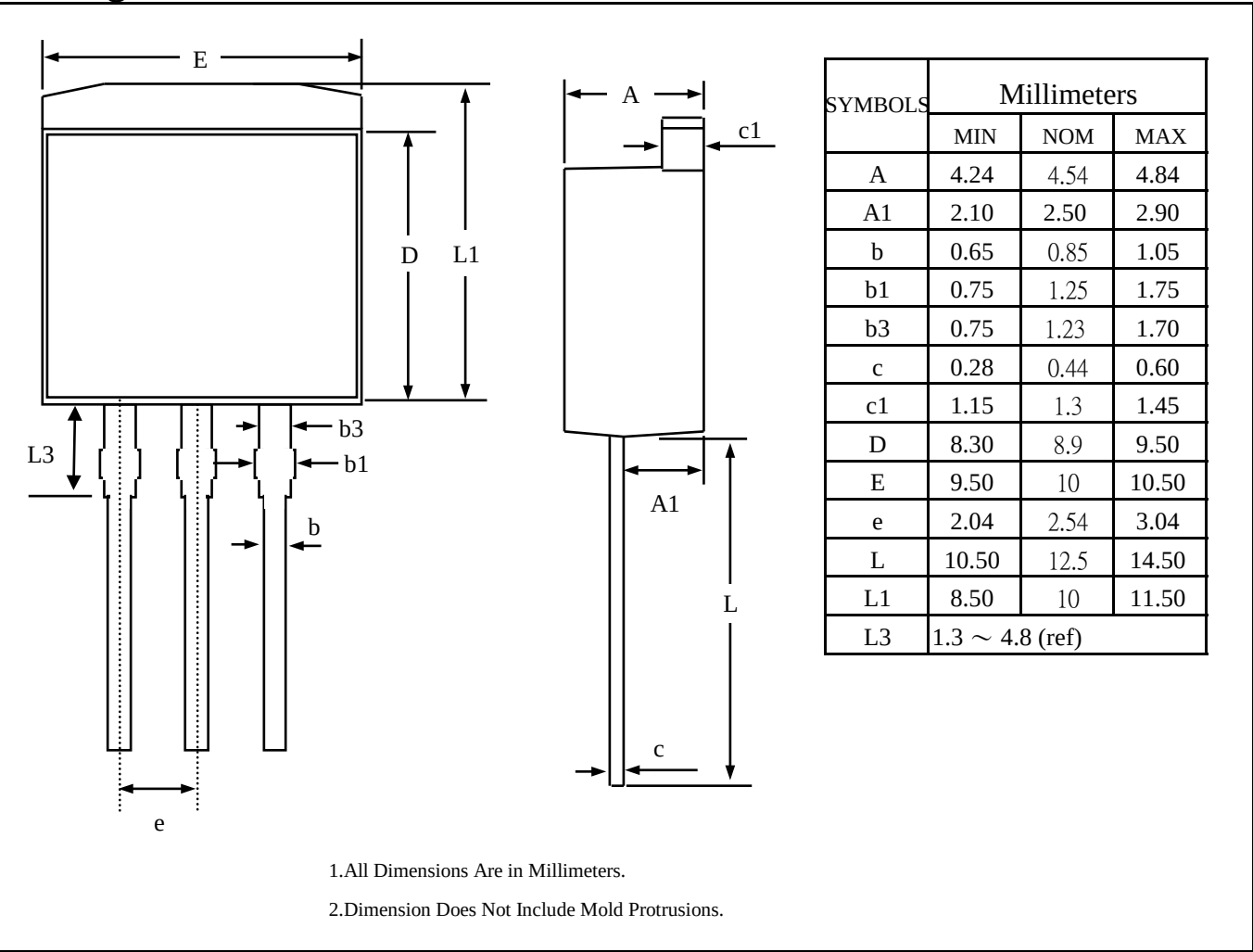


Fig 14. Total Power Dissipation

MARKING INFORMATION

Package Outline : TO-262



TO-262 FOOTPRINT :