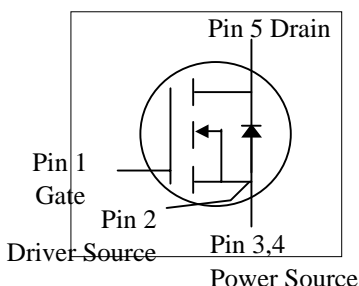


- ▼ 100% R_g & UIS Test
- ▼ Low t_{rr} / Q_{rr}
- ▼ Simple Drive Requirement
- ▼ RoHS Compliant & Halogen-Free

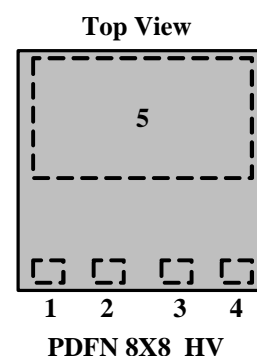


BV _{DSS}	650V
R _{DS(ON)}	0.21Ω
I _D ^{3,4}	19A

Description

XP65SC210D series are innovated design and silicon process technology to achieve the lowest possible on-resistance and fast switching performance. It provides the designer with an extreme efficient device for use in a wide range of power applications.

The PDFN 8X8_HV package is a very low profile for commercial-industrial surface mount application and suited for switching power converters.



Absolute Maximum Ratings @T_j=25°C(unless otherwise specified)

Symbol	Parameter	Rating	Units
V _{DS}	Drain-Source Voltage	650	V
V _{GS}	Gate-Source Voltage	±20	V
V _{GS}	Gate-Source Voltage, AC (f > 1Hz)	±30	V
I _D @T _C =25°C	Drain Current, V _{GS} @ 10V ^{3,4}	19	A
I _D @T _C =100°C	Drain Current, V _{GS} @ 10V ^{3,4}	12	A
I _{DM}	Pulsed Drain Current ¹	44	A
dv/dt	MOSFET dv/dt Ruggedness (V _{DS} = 0 ...480V)	40	V/ns
P _D @T _C =25°C	Total Power Dissipation	138.8	W
P _D @T _A =25°C	Total Power Dissipation ⁷	2.5	W
E _{AS}	Single Pulse Avalanche Energy ⁵	200	mJ
dv/dt	Peak Diode Recovery dv/dt ⁶	15	V/ns
T _{STG}	Storage Temperature Range	-55 to 150	°C
T _J	Operating Junction Temperature Range	-55 to 150	°C

Thermal Data

Symbol	Parameter	Value	Units
R _{thj-c}	Maximum Thermal Resistance, Junction-case	0.9	°C/W
R _{thj-a}	Maximum Thermal Resistance, Junction-ambient ⁷	50	°C/W

Electrical Characteristics @ $T_j=25^{\circ}\text{C}$ (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=1mA$	650	-	-	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance ²	$V_{GS}=10V, I_D=6.2A$	-	-	0.21	Ω
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	2.5	-	4.5	V
g_{fs}	Forward Transconductance	$V_{DS}=10V, I_D=6.2A$	-	10	-	S
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=520V, V_{GS}=0V$	-	-	100	μA
I_{GSS}	Gate-Source Leakage	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 1	μA
Q_g	Total Gate Charge ⁸	$I_D=7.5A$	-	35	56	nC
Q_{gs}	Gate-Source Charge ⁸	$V_{DS}=520V$	-	10	-	nC
Q_{gd}	Gate-Drain ("Miller") Charge ⁸	$V_{GS}=10V$	-	16	-	nC
$t_{d(on)}$	Turn-on Delay Time ⁸	$V_{DD}=300V$	-	15	-	ns
t_r	Rise Time ⁸	$I_D=7.5A$	-	24	-	ns
$t_{d(off)}$	Turn-off Delay Time ⁸	$R_G=5.1\Omega$	-	42	-	ns
t_f	Fall Time ⁸	$V_{GS}=10V$	-	16	-	ns
C_{iss}	Input Capacitance ⁸	$V_{GS}=0V$	-	1360	2176	pF
C_{oss}	Output Capacitance ⁸	$V_{DS}=100V$	-	50	-	pF
C_{rss}	Reverse Transfer Capacitance ⁸	$f=1.0MHz$	-	10	-	pF
R_g	Gate Resistance	$f=1.0MHz$	-	4.5	9	Ω

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{SD}	Forward On Voltage ²	$I_S=6.2A, V_{GS}=0V$	-	-	1.5	V
t_{rr}	Reverse Recovery Time ⁸	$I_S=7.5A, V_{GS}=0V$	-	170	-	ns
Q_{rr}	Reverse Recovery Charge ⁸	$di/dt=100A/\mu s$	-	1.4	-	μC

Notes:

1. Pulse width limited by max. junction temperature.
2. Pulse test
3. Limited by max. junction temperature. Maximum duty cycle $D=0.75$
4. Ensure that the junction temperature does not exceed T_{Jmax} .
5. Starting $T_j=25^{\circ}\text{C}$, $V_{DD}=90V$, $L=100mH$, $R_G=25\Omega$, $V_{GS}=10V$
6. $I_{SD} \leq I_D$, $V_{DD} \leq BV_{DSS}$, starting $T_j = 25^{\circ}\text{C}$
7. Surface mounted on 1 in² copper pad of FR4 board
8. Guaranteed by design.

THIS PRODUCT IS SENSITIVE TO ELECTROSTATIC DISCHARGE, PLEASE HANDLE WITH CAUTION.

USE OF THIS PRODUCT AS A CRITICAL COMPONENT IN LIFE SUPPORT, AUTOMOTIVE OR OTHER SIMILAR SYSTEMS IS NOT AUTHORIZED.

XSEMI DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

XSEMI RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN.

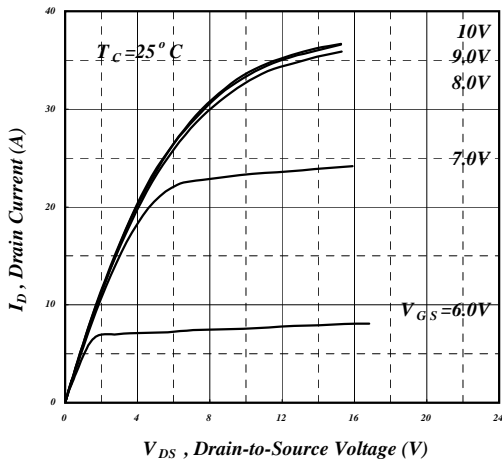


Fig 1. Typical Output Characteristics

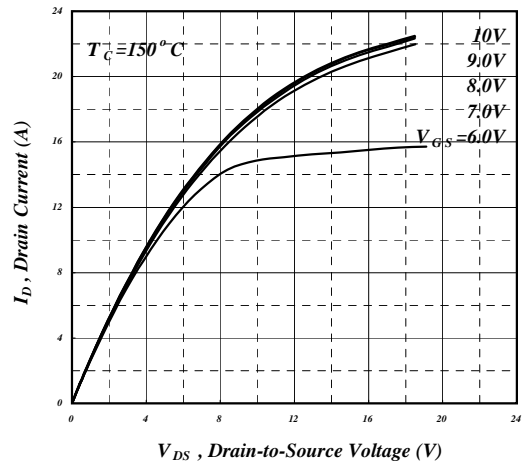


Fig 2. Typical Output Characteristics

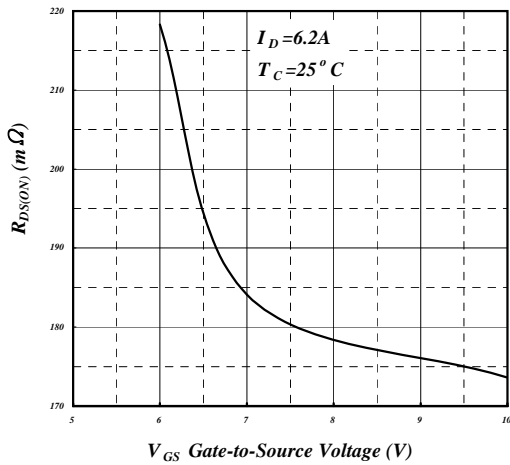


Fig 3. On-Resistance v.s. Gate Voltage

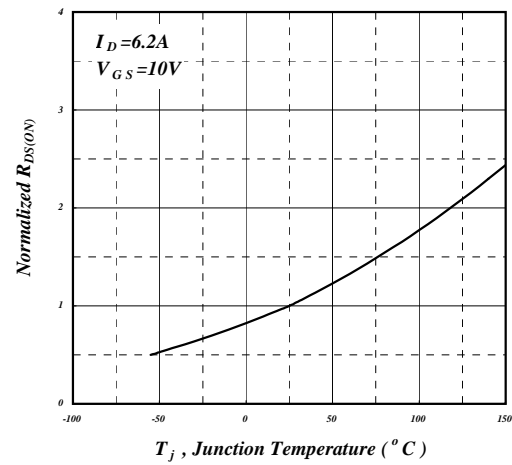


Fig 4. Normalized On-Resistance v.s. Junction Temperature

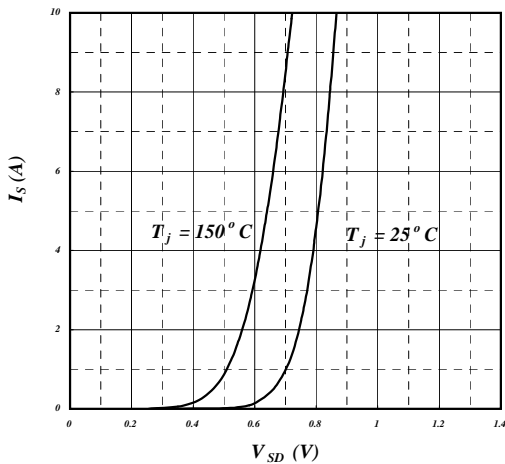


Fig 5. Forward Characteristic of Reverse Diode

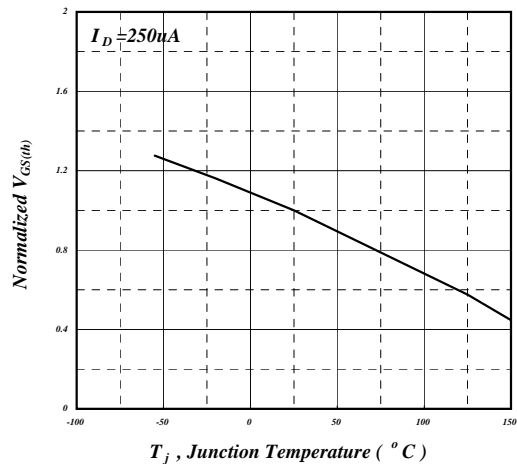


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

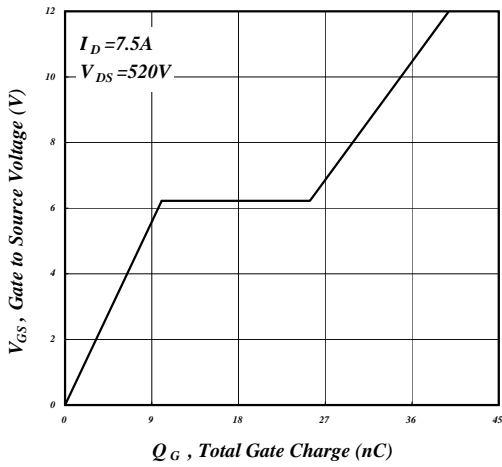


Fig 7. Gate Charge Characteristics

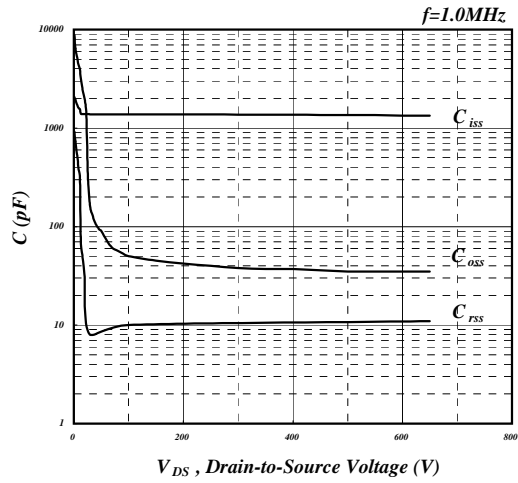


Fig 8. Typical Capacitance Characteristics

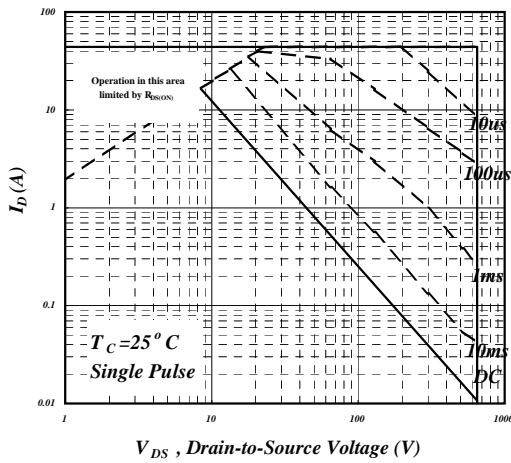


Fig 9. Maximum Safe Operating Area

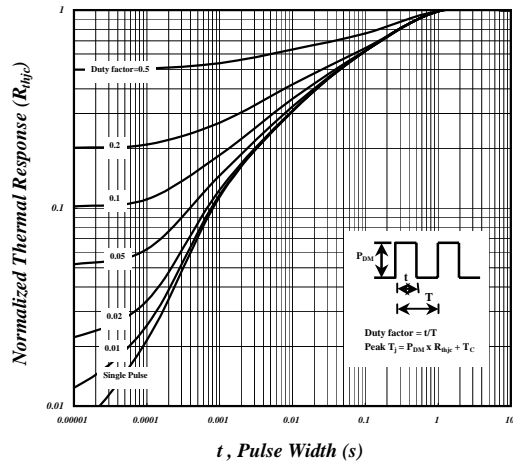


Fig 10. Effective Transient Thermal Impedance

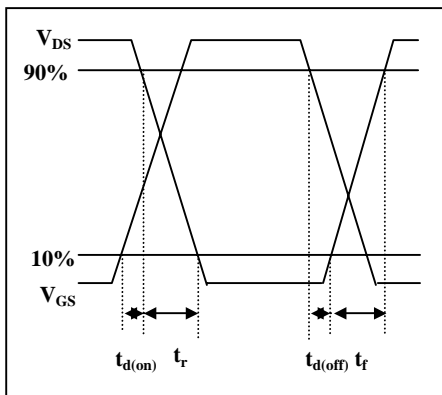


Fig 11. Switching Time Waveform

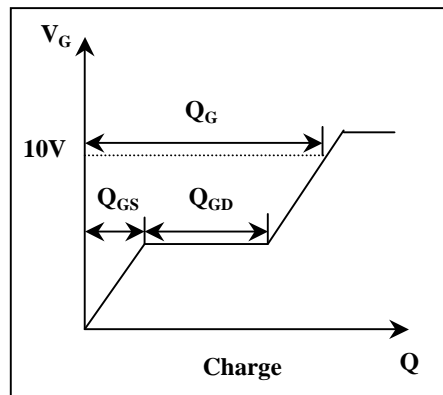


Fig 12. Gate Charge Waveform

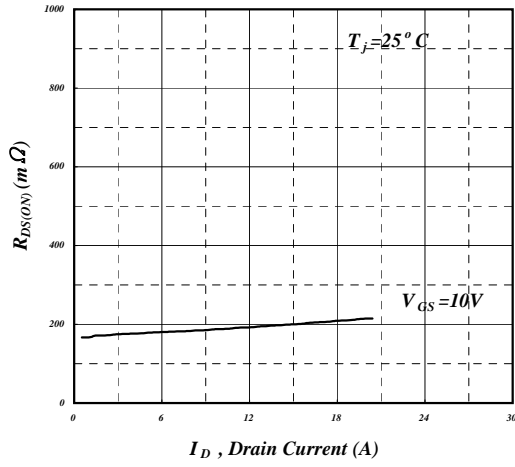


Fig 13. Typ. Drain-Source on State Resistance

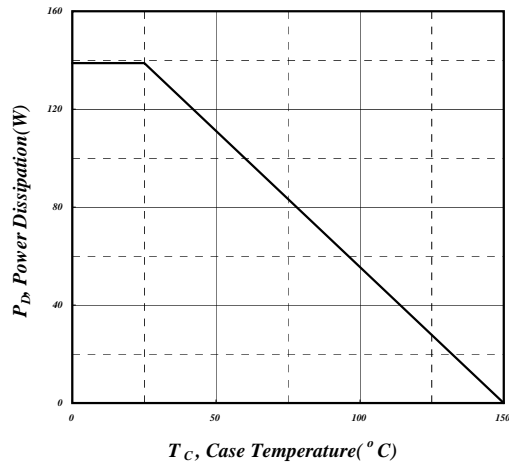
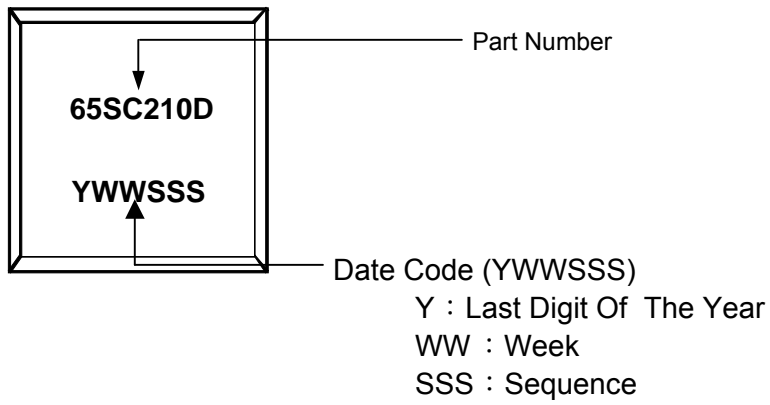
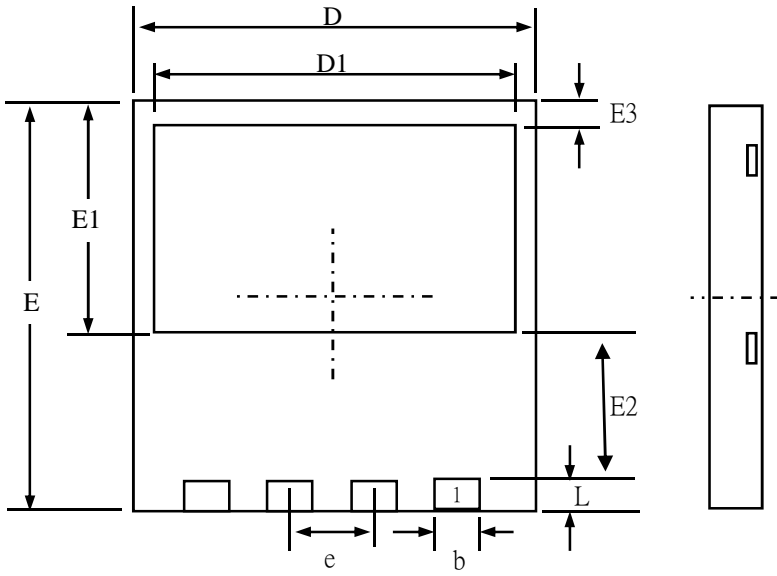


Fig 14. Total Power Dissipation

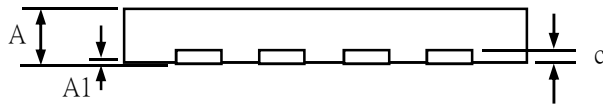
MARKING INFORMATION



Package Outline : PDFN 8x8_HV



BOTTOM VIEW

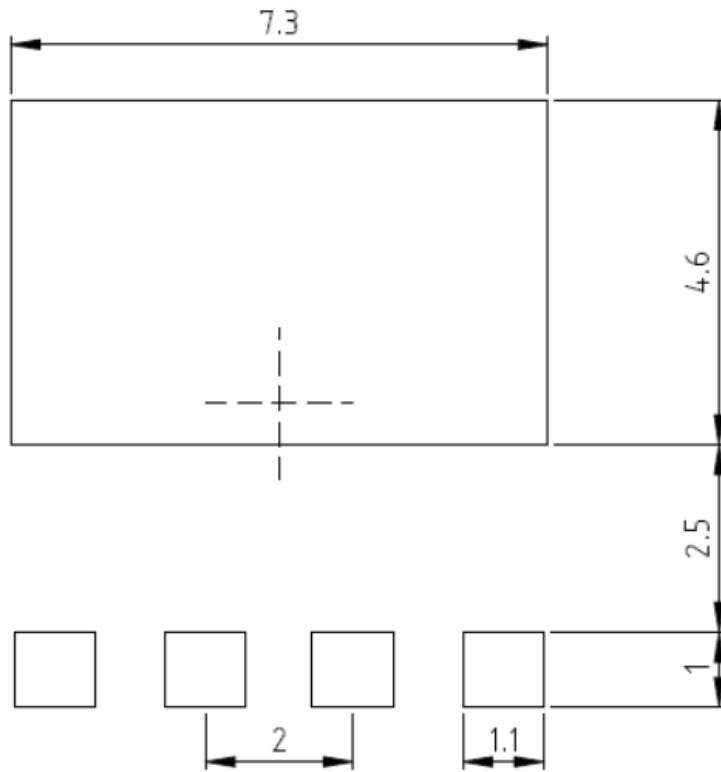


SYMBOLS	Millimeters		
	MIN	NOM	MAX
A	0.75	0.93	1.10
A1	0.00	--	0.05
b	0.90	1.00	1.10
c	0.10	0.20	0.30
D	7.90	8.00	8.10
D1	7.10	7.20	7.30
E	7.90	8.00	8.10
E1	4.25	4.55	4.85
E2	2.65	2.75	2.85
E3	0.30	0.40	0.50
e	2.00BSC		
L	0.40	0.50	0.60

1.All Dimension Are In Millimeters.

2.Dimension Does Not Include Burrs And Mold Flash.

PDFN 8x8 HV FOOTPRINT :



UNIT: mm