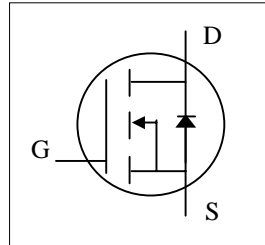


- ▼ 100% R_g & UIS Test
- ▼ Low t_{rr} / Q_{rr}
- ▼ Simple Drive Requirement
- ▼ RoHS Compliant & Halogen-Free

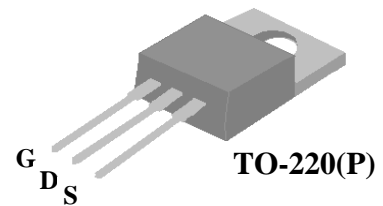


BV _{DSS}	650V
R _{DS(ON)}	99mΩ
I _D ³	38A

Description

XP65SL099D series are innovated design and silicon process technology to achieve the lowest possible on-resistance and fast switching performance. It provides the designer with an extreme efficient device for use in a wide range of power applications.

The TO-220 package is widely preferred for all commercial-industrial through hole applications. The low thermal resistance and low package cost contribute to the worldwide popular package.



Absolute Maximum Ratings @T_j=25°C(unless otherwise specified)

Symbol	Parameter	Rating	Units
V _{DS}	Drain-Source Voltage	650	V
V _{GS}	Gate-Source Voltage	+20	V
V _{GS}	Gate-Source Voltage, AC (f > 1Hz)	+30	V
I _D @T _C =25°C	Drain Current, V _{GS} @ 10V ³	38	A
I _D @T _C =100°C	Drain Current, V _{GS} @ 10V ³	23.5	A
I _{DM}	Pulsed Drain Current ¹	94	A
dv/dt	MOSFET dv/dt Ruggedness (V _{DS} = 0 ...480V)	20	V/ns
P _D @T _C =25°C	Total Power Dissipation	277.8	W
P _D @T _A =25°C	Total Power Dissipation	2	W
E _{AS}	Single Pulse Avalanche Energy ⁴	768	mJ
dv/dt	Peak Diode Recovery dv/dt ⁵	10	V/ns
T _{STG}	Storage Temperature Range	-55 to 150	°C
T _J	Operating Junction Temperature Range	-55 to 150	°C

Thermal Data

Symbol	Parameter	Value	Units
R _{thj-c}	Maximum Thermal Resistance, Junction-case	0.45	°C/W
R _{thj-a}	Maximum Thermal Resistance, Junction-ambient	62	°C/W

Electrical Characteristics @ $T_j=25^{\circ}\text{C}$ (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	650	-	-	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance ²	$V_{GS}=10V, I_D=12.8A$	-	-	99	m Ω
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	2	-	5	V
g_{fs}	Forward Transconductance	$V_{DS}=10V, I_D=12.8A$	-	22	-	S
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=520V, V_{GS}=0V$	-	-	100	μA
I_{GSS}	Gate-Source Leakage	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 1	μA
Q_g	Total Gate Charge ⁶	$I_D=12.8A$	-	113	181	nC
Q_{gs}	Gate-Source Charge ⁶	$V_{DS}=520V$	-	24	-	nC
Q_{gd}	Gate-Drain ("Miller") Charge ⁶	$V_{GS}=10V$	-	48	-	nC
$t_{d(on)}$	Turn-on Delay Time ⁶	$V_{DD}=300V$	-	24	-	ns
t_r	Rise Time ⁶	$I_D=12.8A$	-	39	-	ns
$t_{d(off)}$	Turn-off Delay Time ⁶	$R_G=3.3\Omega$	-	115	-	ns
t_f	Fall Time ⁶	$V_{GS}=10V$	-	35	-	ns
C_{iss}	Input Capacitance ⁶	$V_{GS}=0V$	-	4200	6720	pF
C_{oss}	Output Capacitance ⁶	$V_{DS}=100V$	-	120	-	pF
C_{riss}	Reverse Transfer Capacitance ⁶	$f=1.0\text{MHz}$	-	25	-	pF
R_g	Gate Resistance	$f=1.0\text{MHz}$	-	4.4	8.8	Ω

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{SD}	Forward On Voltage ²	$I_S=12.8A, V_{GS}=0V$	-	-	1.5	V
t_{rr}	Reverse Recovery Time ⁶	$I_S=19.2A, V_{GS}=0V$	-	185	-	ns
Q_{rr}	Reverse Recovery Charge ⁶	$dI/dt=100A/\mu s$	-	1.8	-	μC

Notes:

1. Pulse width limited by max. junction temperature.
2. Pulse test
3. Limited by max. junction temperature. Maximum duty cycle $D=0.75$
4. Starting $T_j=25^{\circ}\text{C}$, $V_{DD}=90V$, $L=150\text{mH}$, $R_G=25\Omega$, $V_{GS}=10V$
5. $I_{SD} \leq I_D$, $V_{DD} \leq BV_{DSS}$, starting $T_j = 25^{\circ}\text{C}$
6. Guaranteed by design.

THIS PRODUCT IS SENSITIVE TO ELECTROSTATIC DISCHARGE, PLEASE HANDLE WITH CAUTION.

USE OF THIS PRODUCT AS A CRITICAL COMPONENT IN LIFE SUPPORT, AUTOMOTIVE OR OTHER SIMILAR SYSTEMS IS NOT AUTHORIZED.

XSEMI DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

XSEMI RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN.

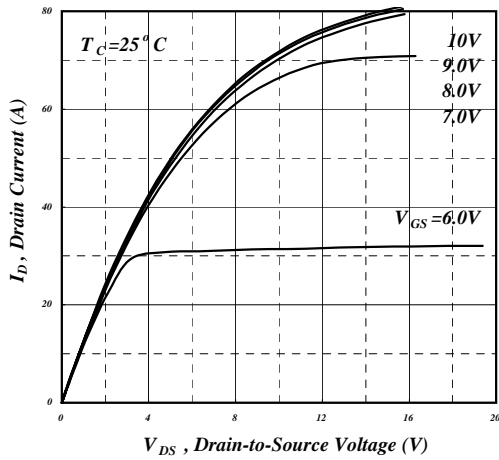


Fig 1. Typical Output Characteristics

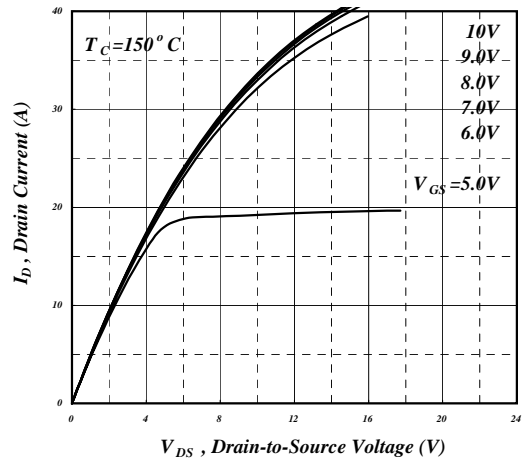


Fig 2. Typical Output Characteristics

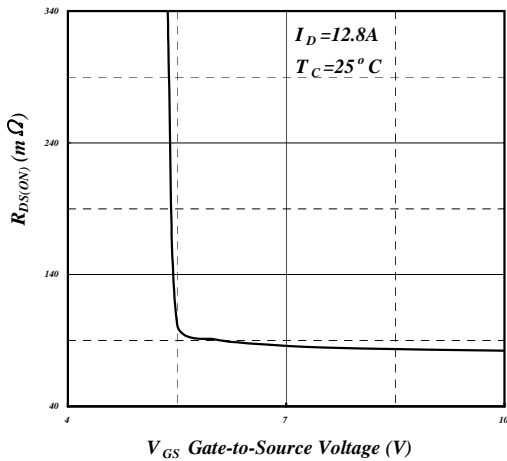


Fig 3. On-Resistance v.s. Gate Voltage

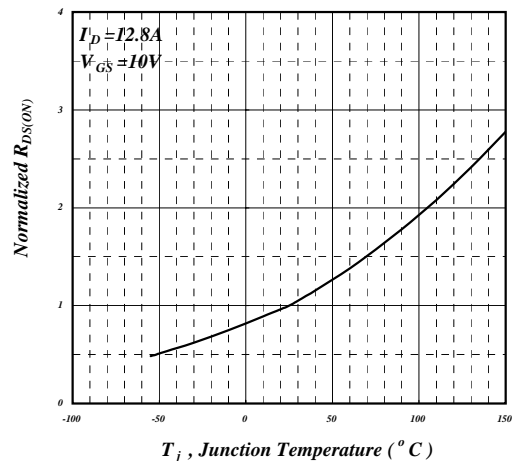


Fig 4. Normalized On-Resistance v.s. Junction Temperature

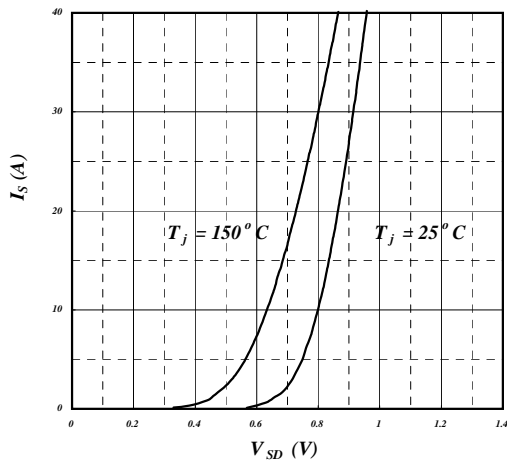


Fig 5. Forward Characteristic of Reverse Diode

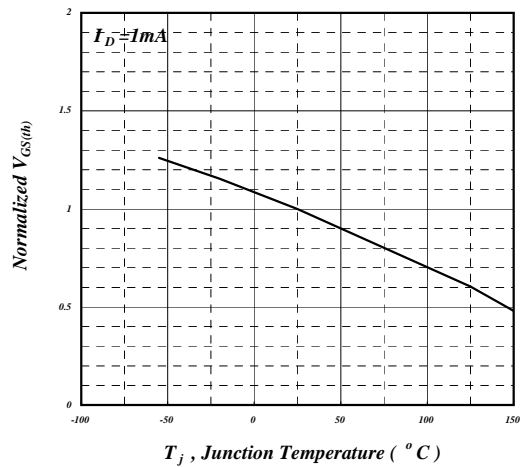


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

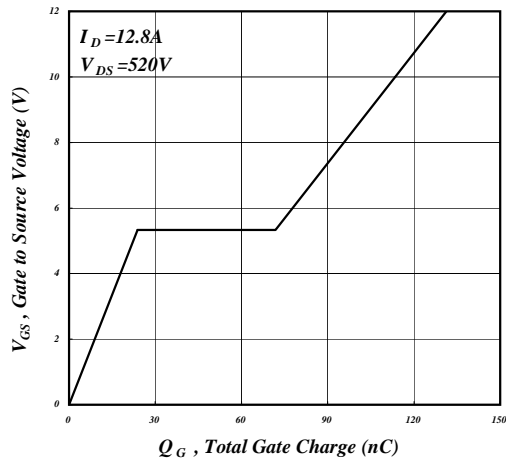


Fig 7. Gate Charge Characteristics

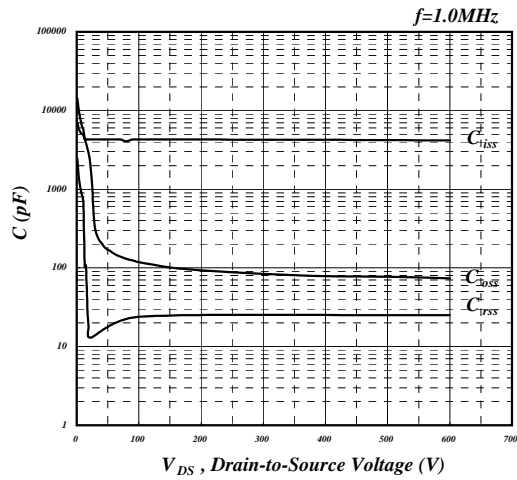


Fig 8. Typical Capacitance Characteristics

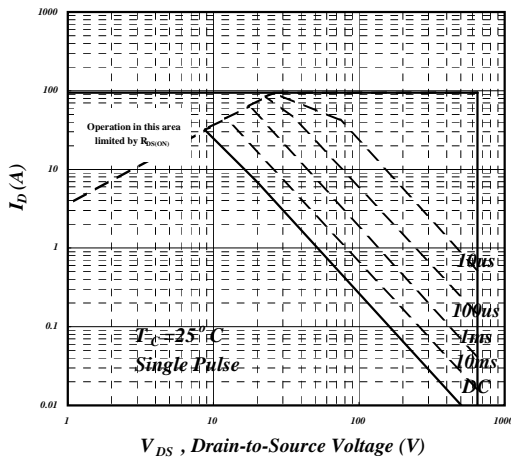


Fig 9. Maximum Safe Operating Area

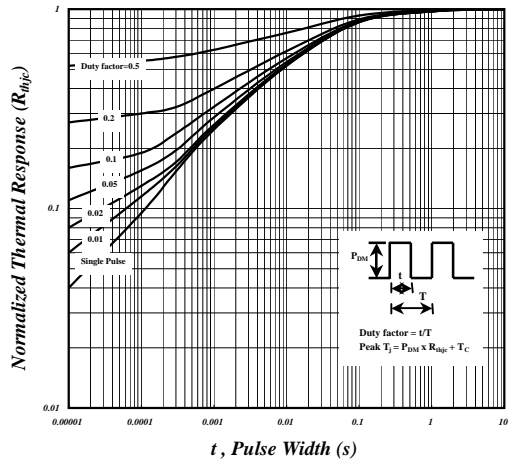


Fig 10. Effective Transient Thermal Impedance

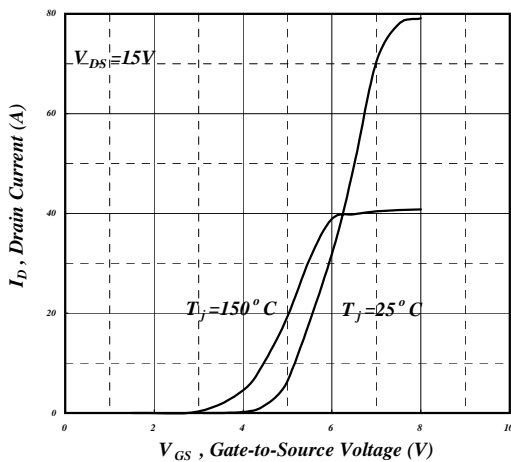


Fig 11. Transfer Characteristics

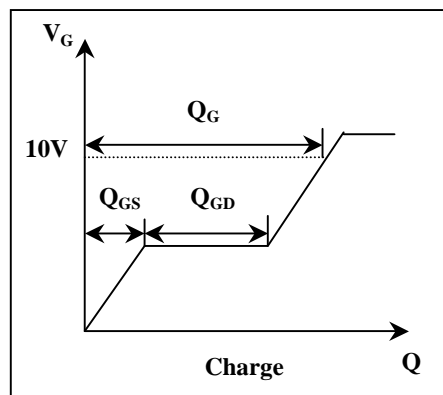


Fig 12. Gate Charge Waveform

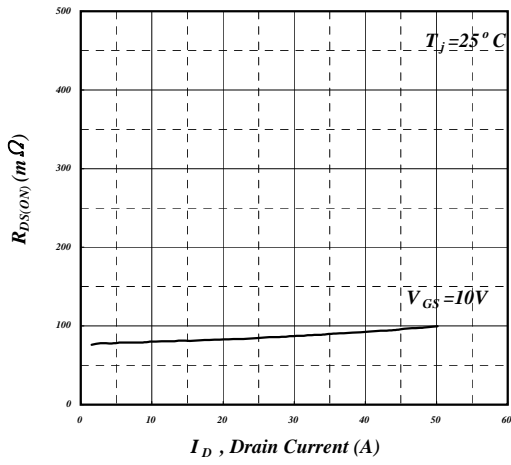


Fig 13. Typ. Drain-Source on State Resistance

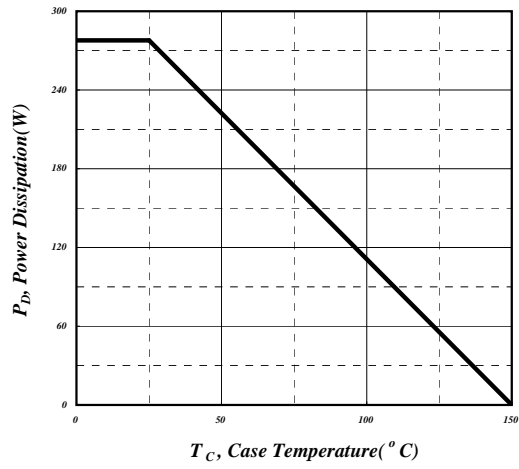
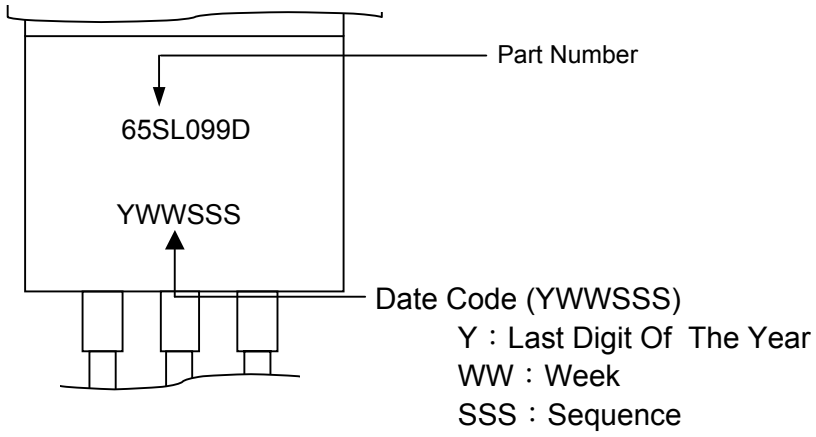
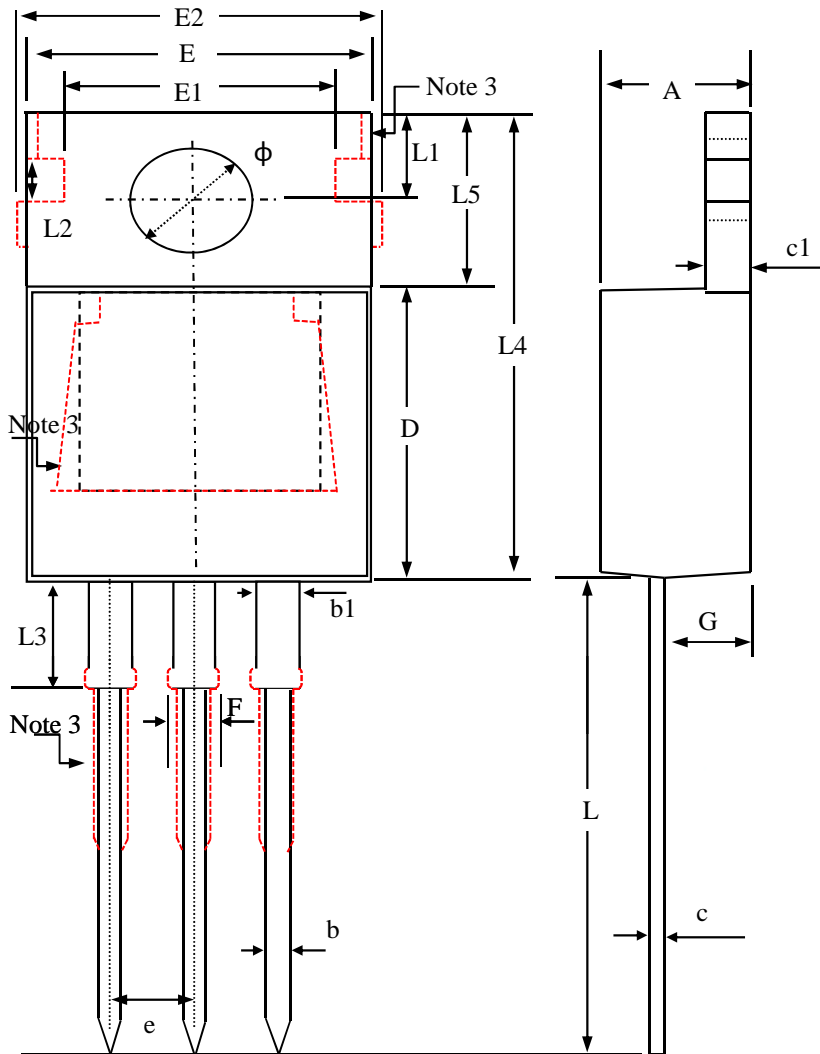


Fig 14. Total Power Dissipation

MARKING INFORMATION



Package Outline : TO-220



SYMBOLS	Millimeters		
	MIN	NOM	MAX
A	4.20	4.50	4.80
b	0.60	0.80	1.00
b1	1.10	1.38	1.80
c	0.30	0.48	0.65
c1	1.10	1.30	1.50
E	9.70	10.00	10.40
E1	7.40	8.30	9.20
e	2.54 (ref.)		
L	12.70	13.60	14.50
L1	2.50	2.75	3.00
L2	1.00	1.40	1.80
L3	2.60	3.35	4.10
L4	14.30	15.15	16.00
L5	6.00	6.40	6.80
ϕ	3.40	3.70	4.00
D	8.30	8.85	9.40
F	1.20	1.41	1.85
G	2.20	2.60	3.00
E2	—	—	11.50

Note:

- 1.All Dimensions Are in Millimeters.
- 2.Dimension Does Not Include Mold Protrusions.
3. Thermal PAD and Pin contour is for reference, it may has little difference by option.

TO-220 FOOTPRINT :

