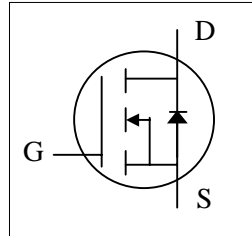


- ▼ 100% R<sub>g</sub> & UIS Test
- ▼ SO-8 Compatible with Heatsink
- ▼ Lower On-resistance
- ▼ RoHS Compliant & Halogen-Free

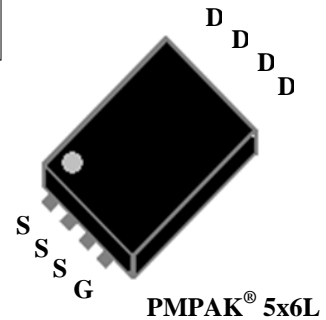


$V_{DSS}$	60V
$R_{DS(ON)}$	6.5m $\Omega$

### Description

XP6NA6R5L series are innovated design and silicon process technology to achieve the lowest possible on-resistance and fast switching performance. It provides the designer with an extreme efficient device for use in a wide range of power applications.

The PMPAK<sup>®</sup> 5x6L package is special for DC-DC converters application and the foot print is compatible with SO-8 with backside heat sink and lower profile.



### Absolute Maximum Ratings @T<sub>j</sub>=25°C (unless otherwise specified)

Symbol	Parameter	Rating	Units
V <sub>DS</sub>	Drain-Source Voltage	60	V
V <sub>GS</sub>	Gate-Source Voltage	±20	V
I <sub>D</sub> @T <sub>C</sub> =25°C	Drain Current, V <sub>GS</sub> @ 10V <sup>5</sup> (Silicon Limited)	68	A
I <sub>D</sub> @T <sub>C</sub> =100°C	Drain Current, V <sub>GS</sub> @ 10V	43	A
I <sub>D</sub> @T <sub>A</sub> =25°C	Drain Current, V <sub>GS</sub> @ 10V <sup>3</sup>	21.6	A
I <sub>D</sub> @T <sub>A</sub> =70°C	Drain Current, V <sub>GS</sub> @ 10V <sup>3</sup>	17.3	A
I <sub>DM</sub>	Pulsed Drain Current <sup>1</sup>	160	A
P <sub>D</sub> @T <sub>C</sub> =25°C	Total Power Dissipation	50	W
P <sub>D</sub> @T <sub>A</sub> =25°C	Total Power Dissipation <sup>3</sup>	5	W
E <sub>AS</sub>	Single Pulse Avalanche Energy <sup>4</sup>	45	mJ
T <sub>STG</sub>	Storage Temperature Range	-55 to 150	°C
T <sub>J</sub>	Operating Junction Temperature Range	-55 to 150	°C

### Thermal Data

Symbol	Parameter	Value	Unit
R <sub>thj-c</sub>	Maximum Thermal Resistance, Junction-case	2.5	°C/W
R <sub>thj-a</sub>	Maximum Thermal Resistance, Junction-ambient <sup>3</sup>	25	°C/W

**Electrical Characteristics @T<sub>j</sub>=25°C(unless otherwise specified)**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =250uA	60	-	-	V
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance <sup>2</sup>	V <sub>GS</sub> =10V, I <sub>D</sub> =13.5A	-	-	6.5	mΩ
		V <sub>GS</sub> =5V, I <sub>D</sub> =11.5A	-	-	11.5	mΩ
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250uA	1.2	-	3	V
g <sub>fs</sub>	Forward Transconductance	V <sub>DS</sub> =5V, I <sub>D</sub> =13.5A	-	29	-	S
I <sub>DSS</sub>	Drain-Source Leakage Current	V <sub>DS</sub> =48V, V <sub>GS</sub> =0V	-	-	25	uA
I <sub>GSS</sub>	Gate-Source Leakage	V <sub>GS</sub> = 20V, V <sub>DS</sub> =0V	-	-	100	nA
Q <sub>g</sub>	Total Gate Charge	I <sub>D</sub> =11.5A	-	28	44.8	nC
Q <sub>gs</sub>	Gate-Source Charge	V <sub>DS</sub> =30V	-	8.5	-	nC
Q <sub>gd</sub>	Gate-Drain ("Miller") Charge	V <sub>GS</sub> =5V	-	13.5	-	nC
t <sub>d(on)</sub>	Turn-on Delay Time	V <sub>DS</sub> =30V	-	13	-	ns
t <sub>r</sub>	Rise Time	I <sub>D</sub> =13.5A	-	39	-	ns
t <sub>d(off)</sub>	Turn-off Delay Time	R <sub>G</sub> =6Ω	-	44	-	ns
t <sub>f</sub>	Fall Time	V <sub>GS</sub> =10V	-	66	-	ns
C <sub>iss</sub>	Input Capacitance	V <sub>GS</sub> =0V	-	2100	3360	pF
C <sub>oss</sub>	Output Capacitance	V <sub>DS</sub> =30V	-	1050	-	pF
C <sub>rss</sub>	Reverse Transfer Capacitance	f=1.0MHz	-	55	-	pF
R <sub>g</sub>	Gate Resistance	f=1.0MHz	-	2	4	Ω

**Source-Drain Diode**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V <sub>SD</sub>	Forward On Voltage <sup>2</sup>	I <sub>S</sub> =13.5A, V <sub>GS</sub> =0V	-	-	1.3	V
t <sub>rr</sub>	Reverse Recovery Time	I <sub>S</sub> =13.5A, V <sub>GS</sub> =0V,	-	31	-	ns
Q <sub>rr</sub>	Reverse Recovery Charge	di/dt=100A/μs	-	20	-	nC

**Notes:**

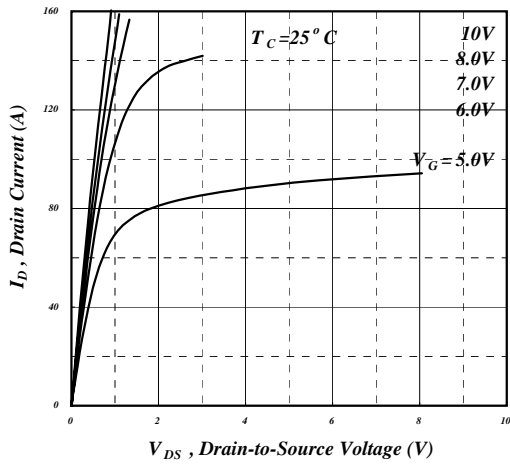
- 1.Pulse width limited by Max. junction temperature.
- 2.Pulse test
- 3.Surface mounted on 1 in<sup>2</sup> copper pad of FR4 board, t ≤10sec; 60°C/W at steady state.
- 4.Starting T<sub>j</sub>=25°C , V<sub>DD</sub>=30V , L=0.1mH , R<sub>G</sub>=25Ω
- 5.Package limitation current is 60A .

THIS PRODUCT IS SENSITIVE TO ELECTROSTATIC DISCHARGE, PLEASE HANDLE WITH CAUTION.

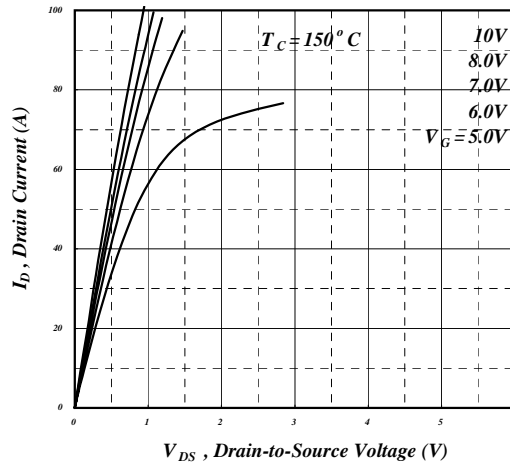
USE OF THIS PRODUCT AS A CRITICAL COMPONENT IN LIFE SUPPORT OR OTHER SIMILAR SYSTEMS IS NOT AUTHORIZED.

XSEMI DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

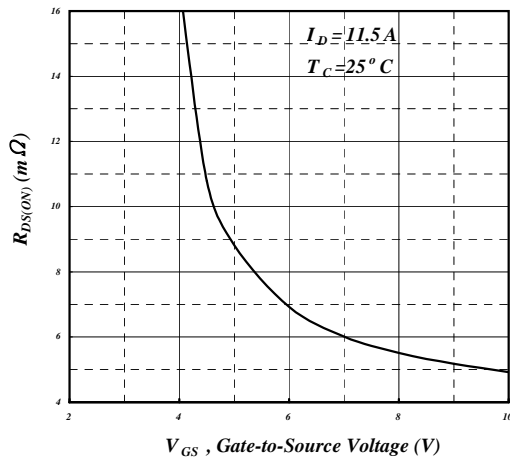
XSEMI RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN.



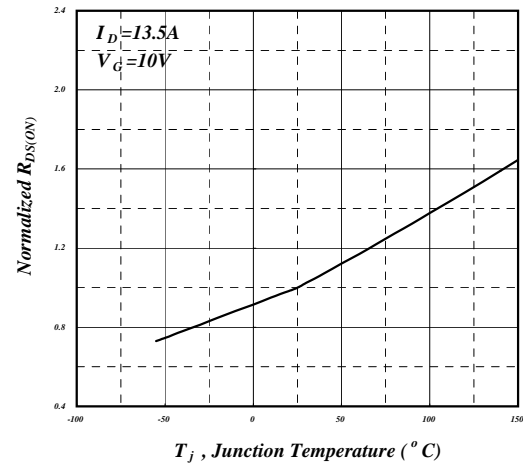
**Fig 1. Typical Output Characteristics**



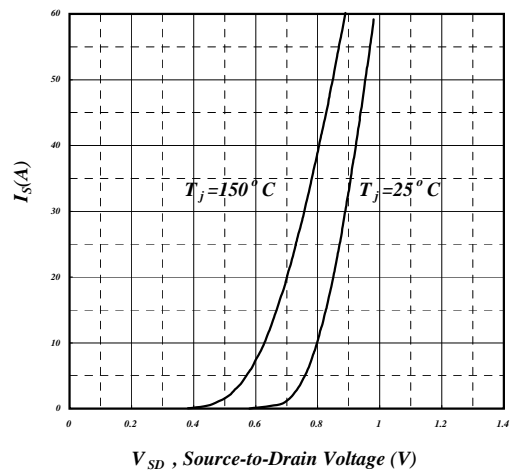
**Fig 2. Typical Output Characteristics**



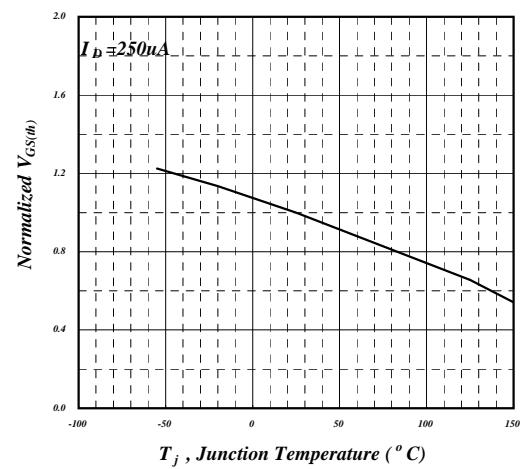
**Fig 3. On-Resistance v.s. Gate Voltage**



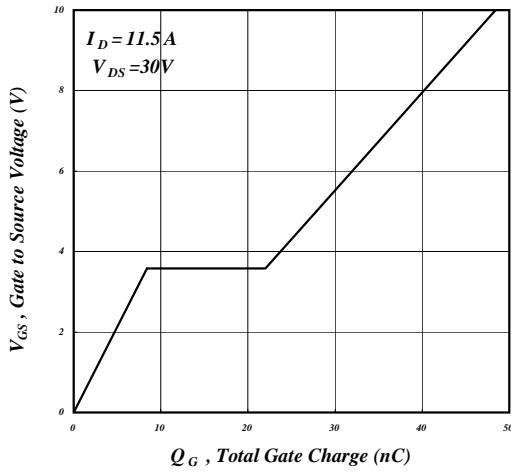
**Fig 4. Normalized On-Resistance v.s. Junction Temperature**



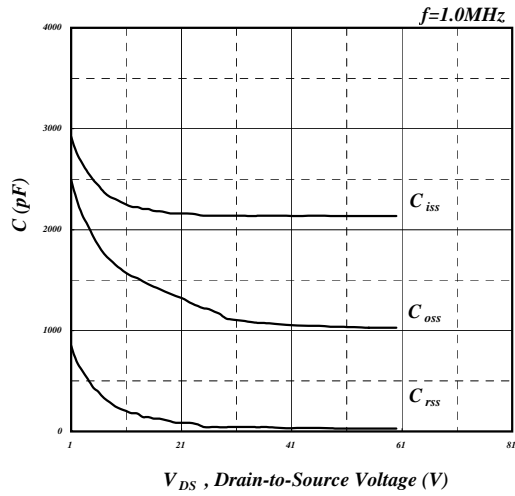
**Fig 5. Forward Characteristic of Reverse Diode**



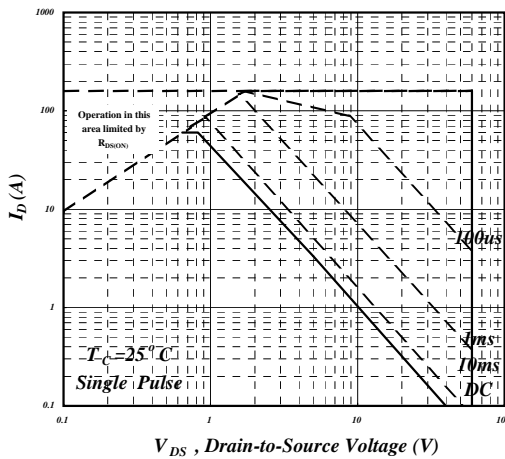
**Fig 6. Gate Threshold Voltage v.s. Junction Temperature**



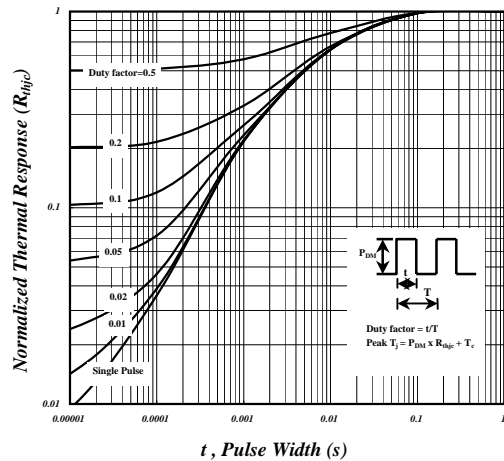
**Fig 7. Gate Charge Characteristics**



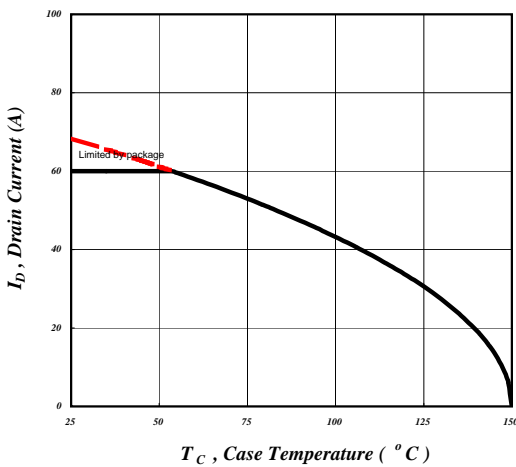
**Fig 8. Typical Capacitance Characteristics**



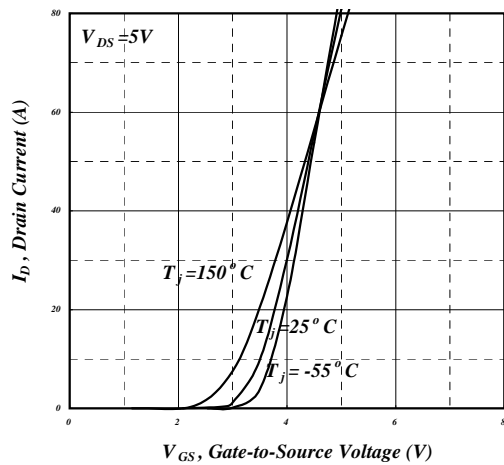
**Fig 9. Maximum Safe Operating Area**



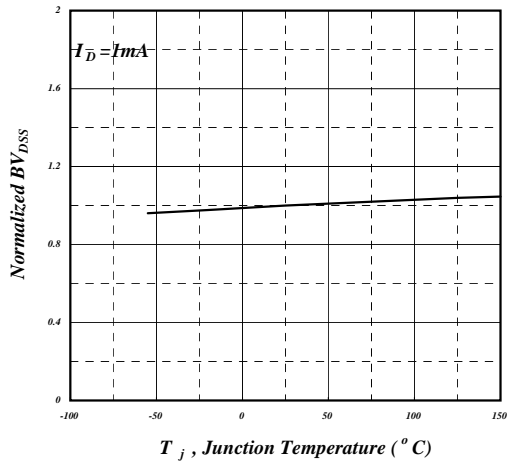
**Fig 10. Effective Transient Thermal Impedance**



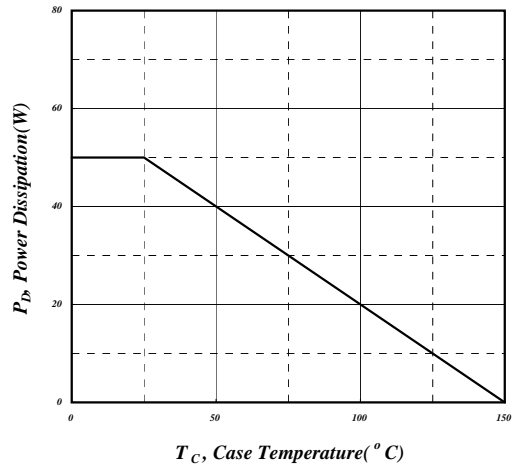
**Fig 11. Drain Current v.s. Case Temperature**



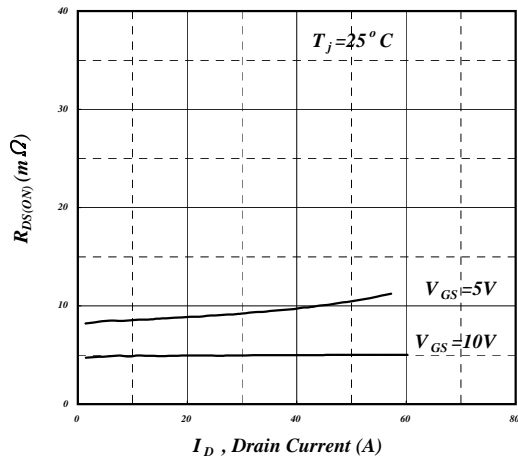
**Fig 12. Transfer Characteristics**



**Fig 13. Normalized  $BV_{DSS}$  v.s. Junction Temperature**



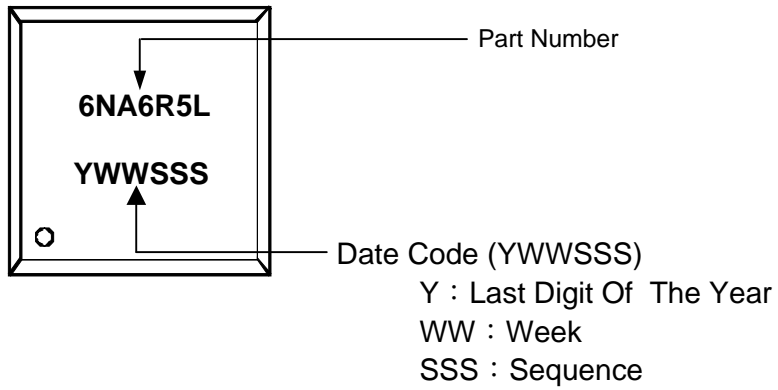
**Fig 14. Total Power Dissipation**



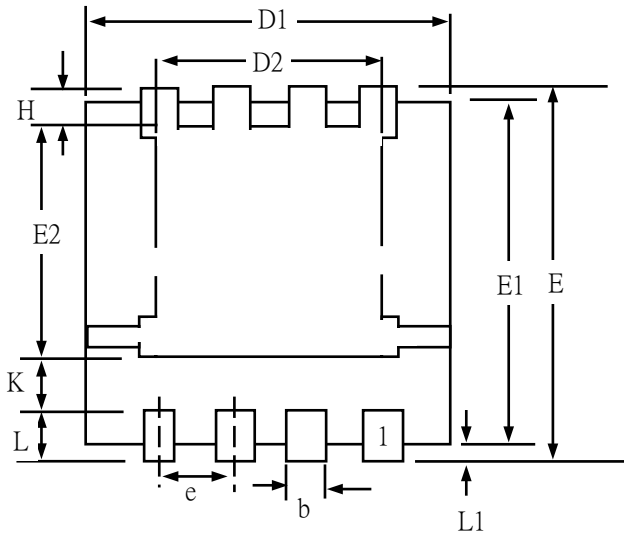
**Fig 15. Typ. Drain-Source on State Resistance**

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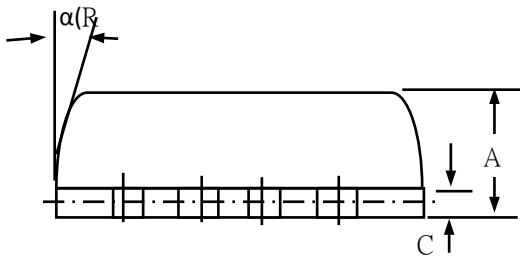
**MARKING INFORMATION**



**Package Outline : PMPAK 5x6L**



BACKSIDE VIEW



SYMBOLS	Millimeters		
	MIN	NOM	MAX
A	0.90	1.10	1.30
b	0.33	0.41	0.51
C	0.15	—	—
D1	4.80	4.90	5.10
D2	3.61	3.81	4.40
E	6.25	6.35	6.45
E1 (Ref.)	5.60	5.75	5.90
E2 (Ref.)	3.30	3.55	3.80
e	1.27 BSC		
H	0.58	0.68	0.90
K (Ref.)	0.70	—	—
L	0.68	0.78	0.88
L1	0.25	0.30	0.40
$\alpha$ (Ref.)	0°	—	12°

- 1.All Dimension Are In Millimeters.
- 2.Dimension Does Not Include Mold Protrusions.

**PMPAK 5X6L FOOTPRINT :**

