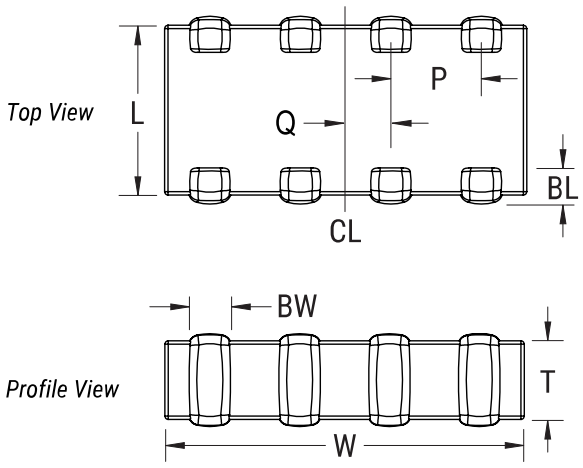
CA0612KRNP09BN101

CA, Ceramic, 100 pF, 10%, 50 VDC, C0G, SMD, MLCC, 0612 / 1632



Click here for the 3D model.

General Information	
Series	CA
Style	SMD Array
Description	SMD, MLCC
Features	Temperature Stable
RoHS	Yes
Termination	Tin
Qualifications	AEC-Q200
MSL	1
Case Code (EIA / mm)	0612 / 1632

Dimensions	
L	1.6mm +/-0.15mm
W	3.2mm +/-0.15mm
T	0.8mm +/-0.1mm
A	0.4mm +/-0.1mm
B	0.3mm +/-0.2mm
P	0.8mm +/-0.1mm

Packaging Specifications	
Packaging	T&R, 178mm, Paper Tape
Packaging Quantity	4000

Specifications	
Capacitance	100 pF
Tolerance	10%
Voltage DC	50 VDC
Temperature Range	-55/+125°C
Temp. Coefficient	C0G
Dissipation Factor	0.1%
Insulation Resistance	5 GOhms

Statements of suitability for certain applications are based on our knowledge of typical operating conditions for such applications, but are not intended to constitute - and we specifically disclaim - any warranty concerning suitability for a specific customer application or use. This Information is intended for use only by customers who have the requisite experience and capability to determine the correct products for their application. Any technical advice inferred from this Information or otherwise provided by us with reference to the use of our products is given gratis, and we assume no obligation or liability for the advice given or results obtained.

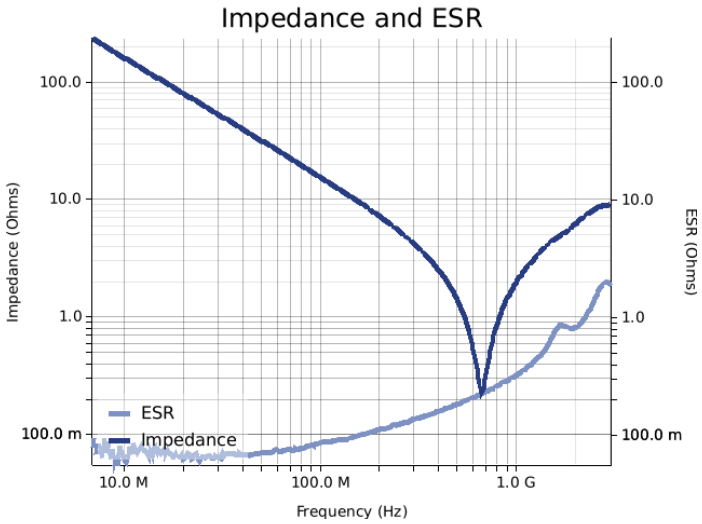
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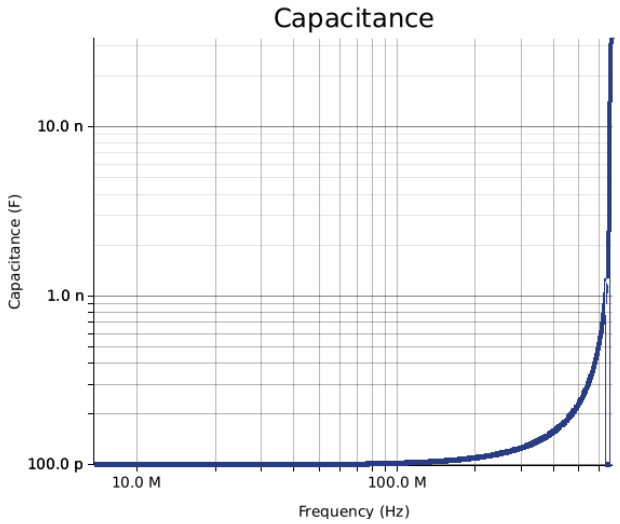
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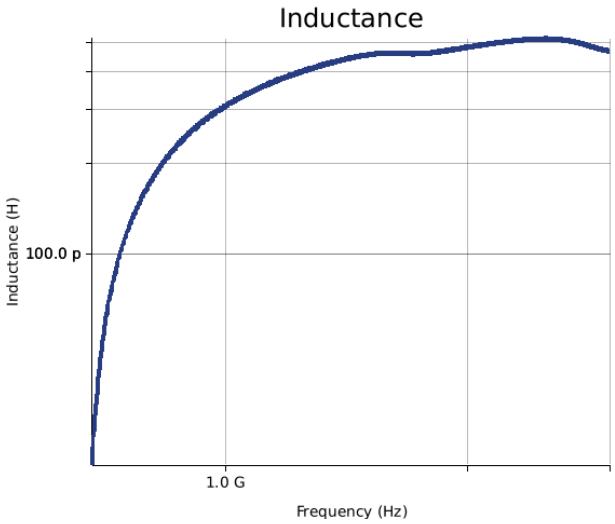
CA, Ceramic, 100 pF, 10%, 50 VDC, C0G, SMD, MLCC, 0612 / 1632

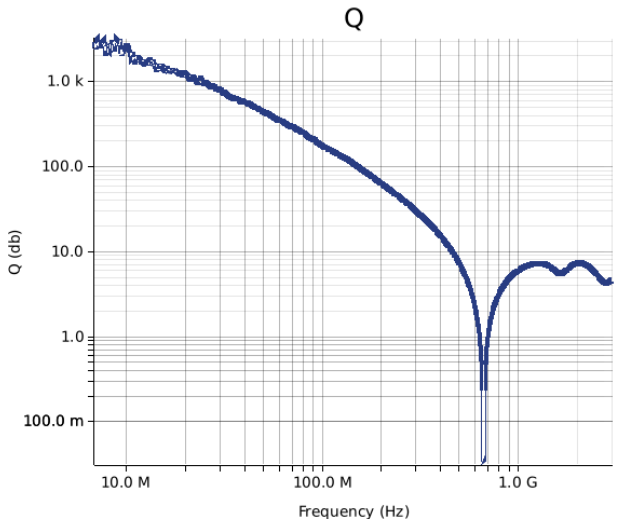
Simulations

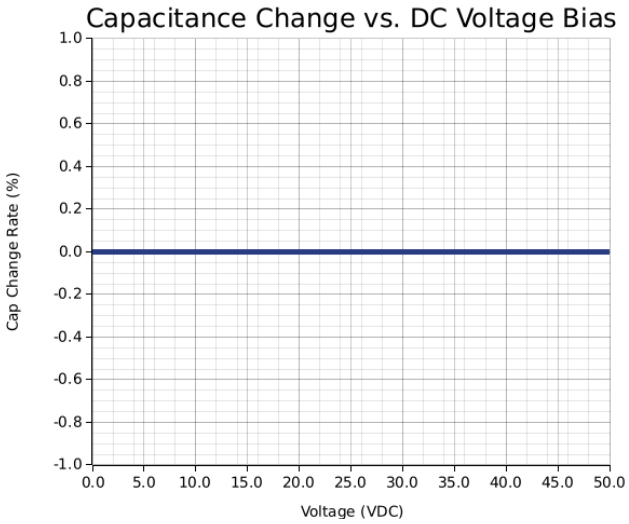
For the complete simulation environment please visit Y-SIM.

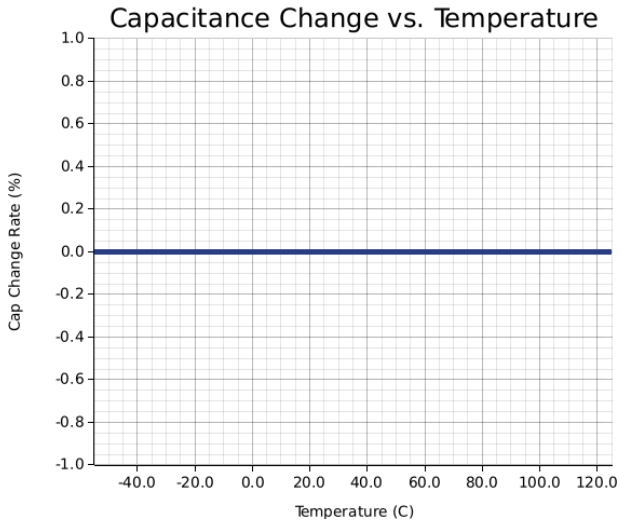








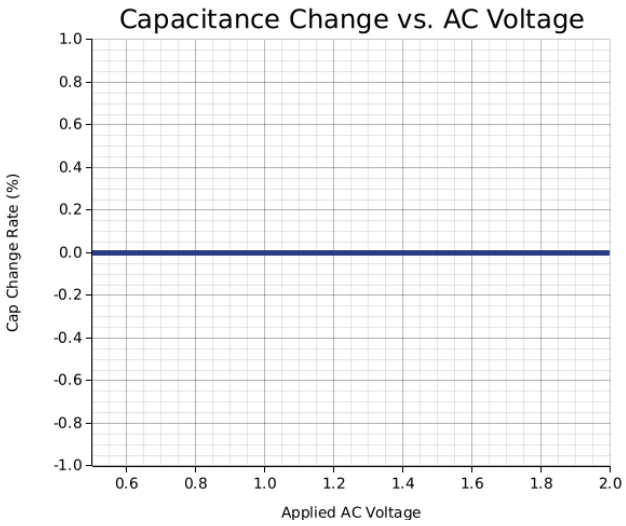


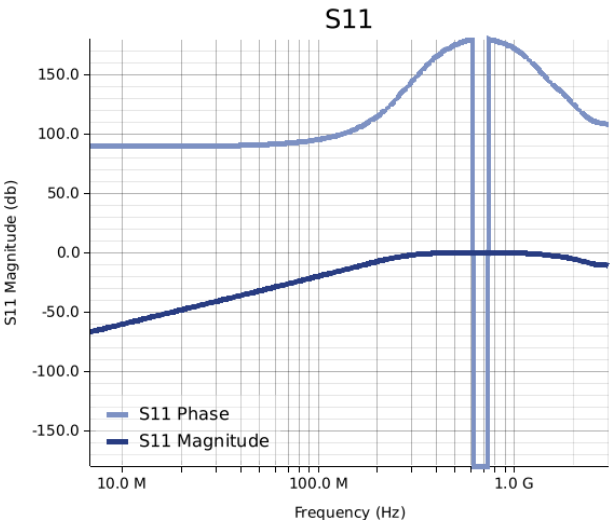


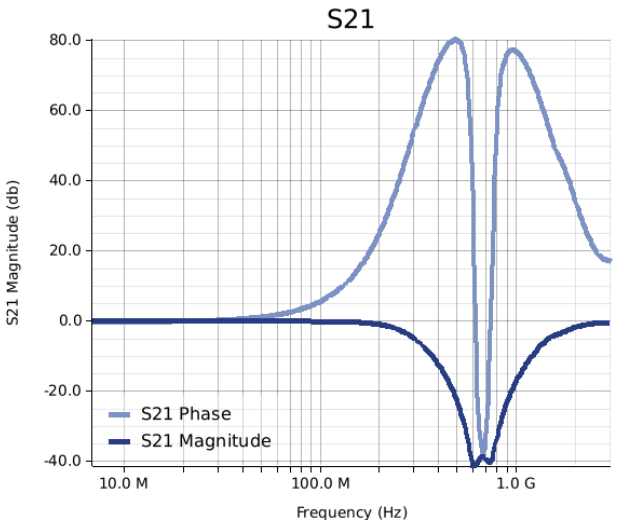
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These are simulations.
This is not a specification!

The responses shown represent the typical response for each part type. Specific responses may vary, depending on manufacturing variation affects of all parameters involved, including the specified tolerances applied to capacitance and unspecified variations of ESR, ESL, and leakage resistance.

The responses shown do not represent a specified or implied maximum capability of the device for all applications.

- The ESR used for ripple “Ripple Current/Voltage vs. Frequency” plots is the ESR at ambient temperature.
- The ESR in the “Temperature Rise vs. Ripple Current” plots is adjusted to each incremental temperature rise before the power and ripple current is calculated.
- The effects shown herein are based on measured data from a multiple part sample of the parts in question.
- Ripple capability of this device will be factored by thermal resistance (Rth) created by circuit traces (addi affects of all parameters involved, including the specified tolerances applied to capacitance and unspecified variations of ESR, ESL, and leakage resistance.
- The peak voltages generated in the “Temperature Rise vs. Combined Ripple Currents” plot are calculated for each frequency and are not combined with voltages generated at any other harmonics.
- Please consult with the catalog or field applications engineer for maximum capability of the device in specific applications.

All product information and data (collectively, the “Information”) are subject to change without notice.

KEMET K-SIM is designed to simulate behavior of components with respect to frequency, ambient temperature, and DC bias levels. The responses shown represent the typical response for each part type. Specific responses may vary, depending on manufacturing variation effects of all parameters involved, including the specified tolerances applied to capacitance and unspecified variations of ESR, ESL, and leakage resistance.

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If you have any questions please contact K-SIM.

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